Broadband Low-Loss Fan-In Chip-to-Package Interconnect Enabling System-in-Package Applications Beyond 220 GHz

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***Abstract*—This paper presents a broadband low-loss fan-in wafer level ball grid array (WLB) vertical through-mold-via (TMV) interconnect that enables highly integrated system-in-package (SiP) applications beyond 220 GHz. The dedicate advantage of the proposed approach is to further minimize the separation between package components (e.g., antenna in package (AiP)) and on-chip receiver or transmitter chain. To demonstrate the robustness of the TMV interconnect design, the necessity for co-simulation of the integrated circuit (IC) package and the IC itself during the package-design is shown. Therefore, an in-depth analysis of the suppression of parasitic mode oscillation inside silicon is carried out. Furthermore, the parasitic radiation loss at the TMV interconnect discontinuity is given and a verification of the proposed TMV due to high agreement of simulation and measurement results is demonstrated. The interconnect has been verified with a measured 10 dB return loss bandwidth of 38 GHz and a de-embedded insertion loss of less than 2.8 dB at 275 GHz, which enables a compact low-loss broadband signal transition from active IC components in the backend-of-line (BEOL) to passive components in package. Compared to fan-out WLB, the developed fan-in WLB solution enables higher integration density of active and passive components with the shortest interconnects for minimal insertion loss. Thus, the proposed fan-in TMV packaging provides a very compact, easy-to-assemble and cost-efficient alternative for SiP designs for future broadband communication and sensing solutions.**

***Index Terms*—Assembly, fan-in WLB (wafer level ball grid array), fan-out WLB, heterogeneous system design, interconnect, signal transition characterization, system-in-package (SiP), wafer level packaging.**

I. INTRODUCTION

THE demand for higher system bandwidth in radar sensing and communication applications is increasing tremendously due to strong demands regarding higher target resolution [1]–[3] or broadband data transfer [4]–[7]. The trend is toward higher frequencies to achieve larger system bandwidth. In particular, for radar sensing applications beyond 220 GHz, a high range resolution, in combination with high angle resolution has various fields of applications, such as high-precision vibration measurements in industrial scenarios [8], vital sign detection [9], and non-destructive or biomedical spectroscopy [3], [10], [11]. The upcoming sub-terahertz communication standard IEEE 802.15.3d in the 300 GHz frequency band provides broadband communication channels for high data-rate exchange in close-proximity communications or intra-device links, thus system solutions have to be developed to utilize this standard [7], [12]. Due to small wavelengths at frequencies beyond 220 GHz, whole system-on-chip (SoC) solutions with receiver and transmitter chains, as well as integrated antennas can be developed [3], [6]. This significantly reduces the form factor and cost of the entire system, enabling the integration of compact and low-cost sensors in applications such as autonomous vehicles, drones, or chip-to-chip communication in data centers [2], [4], [13].

A key component of the system's performance is the design and integration of antennas on-chip. However, a bulky antenna has to be integrated into the expensive IC area, while offering poor radiation efficiency and, thus, low antenna gain due to the chips's naturally low substrate height in the BEOL stackup of the IC processes [14], [15]. This low antenna gain can be compensated for using dielectric lenses, or localized backside etching [1], [7], [16]. However, these techniques require complex system assembly technologies that will increase the system's costs. A remedy is the SiP approach, in which relevant passive components, such as filters, DC-pads, interconnects or antennas, are encapsulated in the IC-package (see Fig. 1) [17].

A. State of the Art Wafer Level Packaging

A major trend in low-cost, highly integrated RF-packaging is the use of wafer level packaging to realize SiP solutions [18]–[25]. Infineon introduced the fan-out WLB, which is referred to embedded wafer level ball grid array (eWLB) [26]. Another fan-out WLB technology, introduced by TSMC, is called integrated fan-out (INFO) package [27], [28]. On the one hand, WLB encapsulates the bare die chip and forms an IC protection. On the other hand, the package serves as a dielectric carrier for passive structures, such as interconnects, filters, or antennas, within the redistribution layer (RDL) [21], [29]. The thin-film RDL can be machined with very high accuracy, enabling precise manufacturing of passive package components [9]. The RDL's high-frequency suitability

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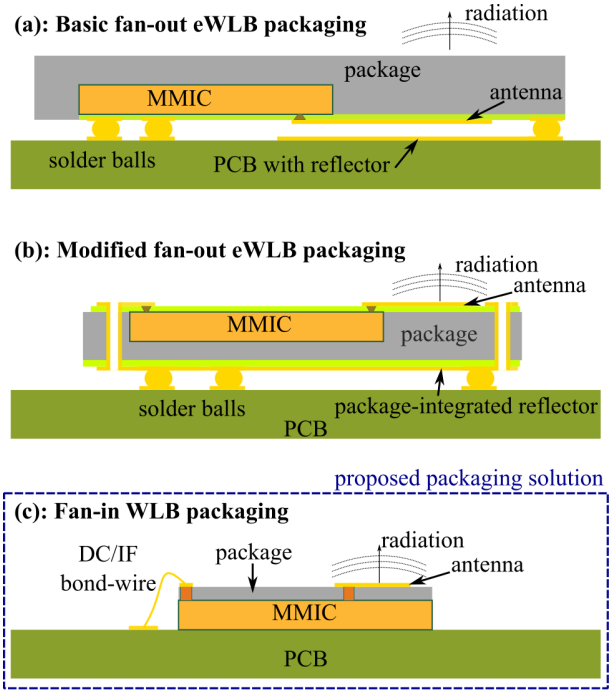

Fig. 1. Comparison of different wafer level packaging topologies.

was thoroughly investigated and demonstrated in [21], [29]. One key advantage compared to other SiP assemblies is the short length of the IC-to-RDL interconnect which enables low parasitic behavior and low-loss signal transition [21]. The state-of-the-art WLB packaging approach eliminates three major limitations of current millimeter-wave (mmW) system design compared to other package assemblies. First, it does not require an interconnect (e.g., a bond-wire) between the IC and PCB, which is required in the quad flat no lead (QFN) system assembly in [8], [30], [31], or in a low-temperature co-fired ceramic (LTCC) packaging, as described in [32], [33]. A bond-wire interconnect at frequencies beyond 220 GHz results in impedance mismatch and performance degradation due to losses [34]. Second, it also eliminates the complex assembly technology required to mount the IC on the PCB and connect it to the off-chip antenna substrate [13]. Third, the integration of the entire system in the eWLB package eliminates the need for an RF-compatible substrate for low-loss power transfer from the IC to the antenna, thereby reducing manufacturing complexity and cost, and in particular avoiding the disadvantages of LTCC structures in terms of shrinkage and layer displacement [2], [13], [35], [36]. Therefore, WLB eliminates three cost drivers in system application design.

The basic eWLB package assembly is shown in Fig. 1(a). The RDL metal layer is used to realize passive components. For eWLB AiP solutions, the ground (GND) metallization on the PCB acts as a reflector for the electrical field. In this setup, different antenna structures in the 77 GHz and 140 GHz frequency range, such as dipoles, patch, vivaldi, or split-ring resonator-based antennas are demonstrated [21], [36]–[38]. Moreover, vertical interconnects for stacked package-on-package (PoP) system applications are shown [22]. As illustrated in Fig. 1(a), the SiP is connected to the PCB via solder balls. The RDL antenna performance highly depends on the distance to GND. A change in height due to process variations in the assembly has dramatic consequences in terms of antenna efficiency, matching, and radiation pattern [9]. As a consequence, a modified eWLB package setup, introduced in [9], is shown in Fig. 1(b). A second RDL metallization layer at the bottom of the package forms a reflector plane for antenna applications. Therefore, the separation between top and bottom RDL layer can be precisely adjusted. Thus, a shift in solder ball height will not influence the performance of the packaged mmW-component. Ring and dipol antennas at 60 GHz, bow-tie antennas and SiP solutions at 130 GHz and 250 GHz are demonstrated in with this package setup in [9], [34] and [2], [35], [39], respectively. However, the modified eWLB packaging has higher costs due to its additional packaging assembly procedure. Furthermore, the RDL components are realized in the fan-out region, so further package miniaturization is required to minimize the separation between package components (e.g., AiP) and receiver or transmitter chain in order to reduce interconnect losses.

B. Proposed Fan-in Wafer Level Packaging

In this paper, a novel packaging approach that minimize the separation between package and IC components for SiP applications beyond 220 GHz is presented. It will result in the lowest insertion loss and increased system integration density due to its vertical packaging approach (see Fig. 1(c)). Within the proposed fan-in packaging, the RDL structures, such as antennas or transmission lines, are no located beside the IC but directly above it. The IC itself determines the overall dimensions of the SiP, and thus, the form-factor is highly reduced compared to assemblies as shown in Fig. 1(b). Moreover, the IC serves as the GND layer for the RDL structures, so only one RDL layer is required, which reduces the assembly complexity compared to that shown in Fig. 1(b). In addition, the chip integration density can be further increased in this fan-in packaging setup, since non-RF-sensitive circuits, such as analog-, mixed-signal, or digital blocks, can be placed underneath the packaging components, e.g., below the AiP. However, a robust, low-loss, and compact fan-in TMV signal transition from the BEOL to RDL has to be developed first before SiP solutions with RDL-integrated antennas, couplers, or interconnects for chip-to-chip communication can be realized with the proposed packaging approach. Therefore, this paper focuses on the transition development, in-depth simulations in terms of robustness, and metrological verification, to demonstrate the capability of this packaging approach.

This paper is organized as follows. In Section II, the layer stackup of the proposed packaging approach is shown. The assembly and the manufacturing process are presented in Section III. Section IV focuses on the optimization of the interconnect in terms of its robustness, parasitic radiation, and suppression of mutual coupling. The measurement setup and the comparison of simulated and measured results are discussed in Section V. This paper is concluded in Section VI.

II. FAN-IN PACKAGE LAYER STACKUP

Fig. 2 shows the BEOL layer stackup of the Infineon SiGe BiCMOS B11HFC technology, including the fan-in through-mold-via (TMV) interconnect. The BEOL consists of six copper layers and an aluminum layer on top, resulting in a total height of about $9.5\,\mu m$. A copper pillar is plated on top of BEOL, which is encapsulated in the mold compound (MC). In contrast to existing packaging interconnects, the copper pillar is not conical, but cylindrical, and forms the interconnection between BEOL and package topside. The process chain for the manufacturing of the pillars is described in Section III.

The diameter of the TMV, d_{TMV}, is $50\,\mu m$ and the height, h_{TMV}, is $40\,\mu m$, resulting in an aspect ratio of 1:1.2. Compared to existing TMVs in [22] or in [40] the diameter d_{TMV} was reduced significantly from $150\,\mu m$ to $50\,\mu m$. This aspect ratio optimization was necessary to make the TMV suitable for high performing sub-THz SiP applications. The selection of the TMV height and diameter resulting from the aspect ratio, has been studied in detail in 3D-EM simulations. On the one hand, the achieved height $h_{TMV} = 40\,\mu m$ is sufficient for the implementation of fan-in antennas with high radiation efficiency, on the other hand, the resulting diameter of the TMV, due to the underlying aspect ratio, is still small enough to keep the parasitic effects low. This is a trade-off between RF performance and manufacturability. On top of the MC, the RDL is made of copper with a conductor height of $8\,\mu m$ and is used for structuring transmission lines, contact pads, couplers, interconnects, or antennas-in-package (AiP). The MC serves as a dielectric layer between RDL and BEOL.

The proposed package stackup is particularly advantageous for the performance of AiPs due to the increased separation of antenna and the GND, which maximizes the antenna's matching bandwidth, radiation efficiency, and antenna gain [41], compared to those with on-chip antennas (AoCs), as shown in Fig. 3. Both the realized antenna gain and the matching bandwidth are increased. The proposed packaging achieves a matching bandwidth of $20\,GHz$ and an antenna gain of around $5\,dBi$ compared to $3\,GHz$ and $1.2\,dBi$ with AoC.

To validate the TMV transition for further AiP applications,

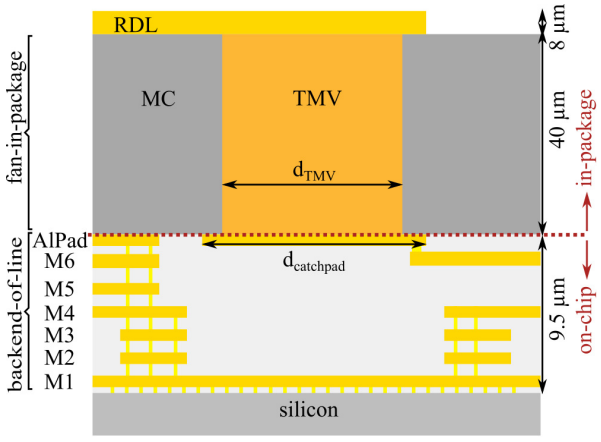

Fig. 2. Layer stackup of the BEOL process and the fan-in TMV interconnect with RDL transmission line on top of the MC-package (not to scale).

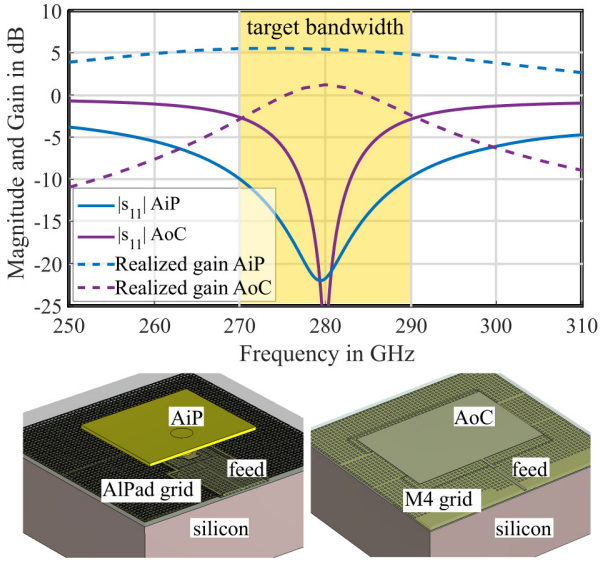

Fig. 3. Simulated antenna performance comparison of AiP with proposed packaging and BEOL AoC.

the following layer stackup is used. The catchpad for the TMV implemented on the AlPad layer has a diameter $d_{catchpad}$ of $60\,\mu m$ (see Fig. 2). To ensure sufficient margin in the package assembly procedure, $d_{catchpad}$ has to be larger than the pillar diameter d_{TMV}. The microstrip line (MSL) in BEOL is made by metal layer M6 (signal) and M4 (GND) forming an impedance of $50\,\Omega$. Underneath the catchpad, the GND layer has been reduced from M4 to M1 to decrease the capacitance between the two metal layers (see detailed analysis in Section IV).

III. ASSEMBLY OF THE FAN-IN WAFER LEVEL PACKAGE

The process and manufacturing chain of the TMV interconnect are shown in Fig. 4. Within this figure, a distinction is made between the wafer level, where the entire wafer is processed, and the unit level, after mechanical dicing and separation of the packaged ICs. The TMV is made of copper via spin-coat resist, structuring, and electroplating. The TMV height is defined by the electric current density, the chip

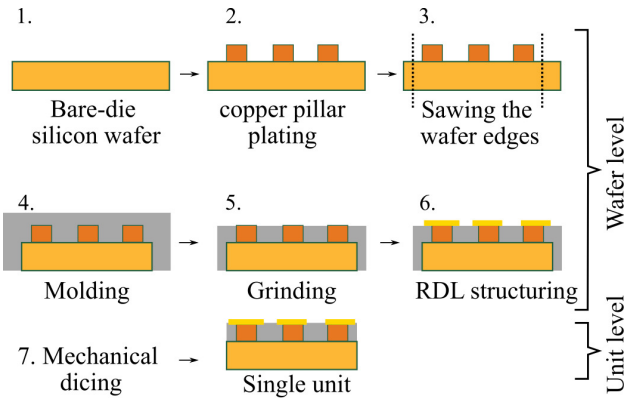

Fig. 4. Process chain of the fan-in TMV interconnect packaging.

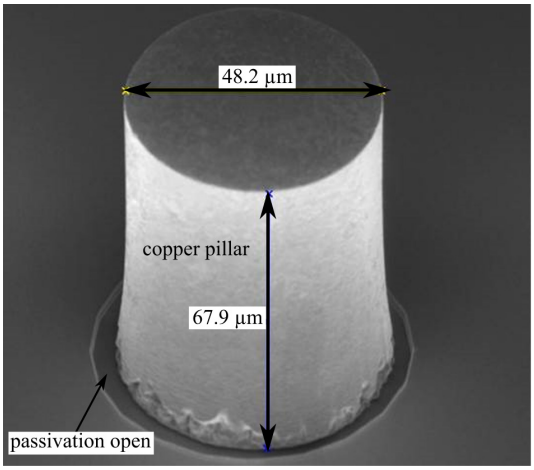

Fig. 5. Scanning electron microscopy of the copper pillar after plating.

area where the plating is to be performed, and the plating duration (the second step in Fig. 4). The shape of the TMV is not conical but that of a cylindrical copper pillar and is defined by the shape of the photoresist. This allows for uniform thickness of the copper pillars, as shown in Fig. 5. Moreover, copper pillars enable a finer pitch than solder ball interconnects do, which allow for higher interconnect density. After pillar plating, the wafer diameter is reduced by mechanical wafer edge sawing (third step) and afterwards the silicon wafer is overmolded using a compression mold process (fourth step). The copper pillars are exposed by back-grinding, and the desired MC thickness is determined (fifth step). The transmission structures on top of the MC are realized within the RDL layer made of copper (sixth step). Therefore, BEOL is connected to RDL with the TMV interconnect for fan-in WLB SiP applications. The edge of the IC is the same as the edge of the package after mechanical dicing (seventh step) of the wafer and separation of the wafer to single packaged chips. The cross-section of the assembled TMV structures is shown in Fig. 6.

IV. DESIGN AND OPTIMIZATION OF A LOW-LOSS AND ROBUST FAN-IN TMV INTERCONNECT

A. Silicon Shielding in the BEOL Stackup

In this section, a detailed analysis of the robustness, parasitic radiation, and cross-coupling between adjacent TMV interconnects is presented. As illustrated in Fig. 2, the silicon

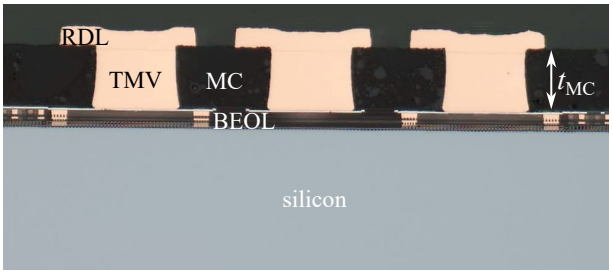

Fig. 6. Microscope cross-section of assembled and packaged TMV interconnects.

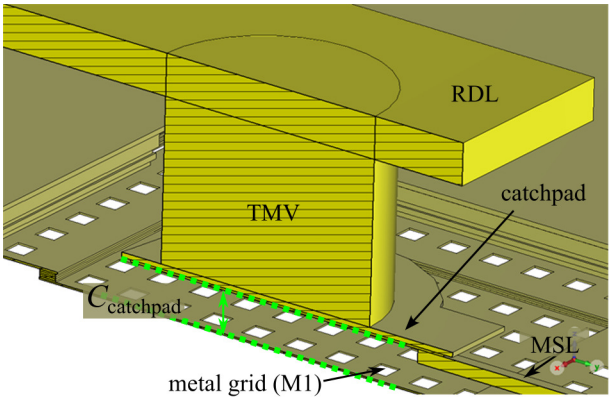

Fig. 7. Cross-section of the TMV interconnect with catchpad and metal grid for silicon shielding (all dielectric layers are transparent).

is shielded by a metal grid on M1 layer. This is counter-intuitive at first, since the small separation of the catchpad on AlPad layer and GND on M1 causes a high parasitic capacitance C_{catchpad} (see Fig. 7), which reduces the achievable bandwidth performance. Without the metal grid on M1 below the catchpad, part of the electric field couples into the silicon through the open metal M1 below the catchpad. The coupling through the M1 apertures is illustrated in Fig. 8 in the cross-section of the back-to-back (b-t-b) simulation model. B-t-b refers to the double transition from the RDL via TMV to the BEOL via TMV to the RDL. A part of the transmitted power is lost during the transition from RDL layer to the BEOL and vice versa. At frequencies beyond 220 GHz, the guided wavelength λ_{guided} with relative permittivity ε_r = 11.9 within the semi conducting silicon is below 400 µm. The signal coupling into the silicon excites parasitic modes inside the silicon substrate. The boundary conditions are defined by the metallic and dielectric boundaries at the respective silicon interfaces. A metallic boundary is formed at the bottom of the silicon due to a metallic chuck in on-wafer measurements or metallized PCB of the carrier board (see Fig. 8). In either case, it is important to provide a conductive layer below the IC that connects a sufficient heat sink directly to the chip to reduce heat generation due to power dissipation within the IC. On top of the silicon is the BEOL, with several metallization layers (see Fig. 2) that represent a metallic boundary condition for the excitation of the parasitic modes in

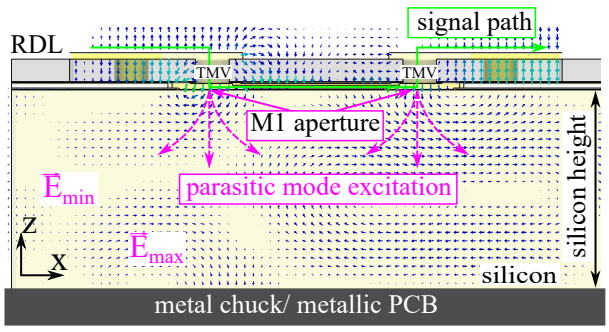

Fig. 8. Parasitic box mode excitation inside silicon due to missing metal M1 shielding below the catchpad (cross-section of the btb simulation).

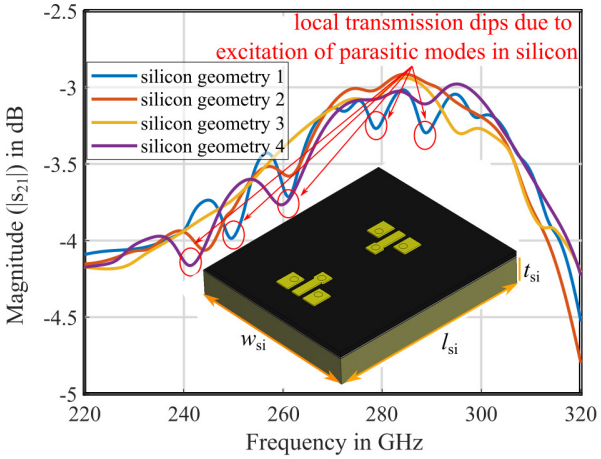

Fig. 9. Silicon geometry dependent transmission characteristics with dips due to excitation of box modes inside silicon (without silicon shielding).

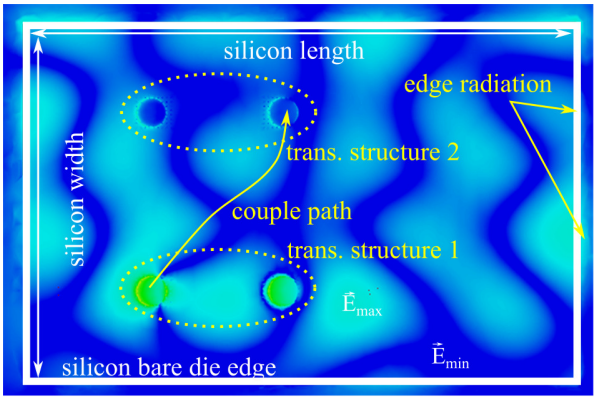

Fig. 10. Topview of the parasitic box mode oscillation inside silicon with parasitic couple path and disturbing lateral radiation on silicon edge due to excitation of transmission structure 1.

the positive z-direction (see Fig. 8). The lateral boundaries are defined as a permittivity discontinuity from silicon (ε_r = 11.9) to air ($\varepsilon_r \approx 1$). Due to the prevailing boundary conditions, parasitic modes as parallel plate modes (PPM), surface waves, and box modes can be excited within the silicon. Contrary to other modes, the TM_0 has no cutoff frequency, allowing the mode to propagate at 0 GHz. Moreover, the silicon width, height and length determine the number and types of parasitic modes inside the silicon. The cutoff frequency of PPM, such as $TM_{PPM,n}$ and $TE_{PPM,n}$ is given in [42]

$$f_{TM_{PPM,n}} = f_{TE_{PPM,n}} = \frac{n}{2 \cdot t_{si} \cdot \sqrt{\mu_0 \varepsilon_0 \varepsilon_r}}\ ,\ n = 1, 2, 3, \ldots\ . \quad (1)$$

The cutoff frequency of $TM_{PPM,1}$ and $TE_{PPM,1}$ with a silicon thickness t_{si} of 185 µm and ε_r of 11.9 is equal to 235 GHz.

In addition, in chip areas without solid metal layer in the BEOL, dielectric slab modes (DSMs) can propagate in the silicon. The cutoff frequency of the TM DSMs is given in [42]

$$f_{TM_{DSM,n}} = \frac{n \cdot c_0}{2 \cdot t_{si} \cdot \sqrt{\varepsilon_r - 1}}\ ,\ n = 0, 1, 2, \ldots \quad (2)$$

with the speed of light in vacuum c_0. In the frequency band of interest, $TM_{DSM,0}$ and $TM_{DSM,1}$ can propagate beyond 0 GHz and 246 GHz, respectively. The cutoff frequency of the TE dielectric slab modes is defined by [42]

$$f_{c_{TE_{DSM,n}}} = \frac{(2n-1) \cdot c_0}{4 \cdot t_{si} \cdot \sqrt{\varepsilon_r - 1}}\ ,\ n = 1, 2, 3, \ldots\ . \quad (3)$$

Within the frequency band of interest $TE_{DSM,1}$ mode can propagate beyond 123 GHz. Overall, several parasitic modes can propagate inside the silicon within the frequency band of interest [41], [43], [44]. The application of through-silicon-vias as a via-fence to suppress substrate modes is unsuitable because of additional manufacturing, assembly complexity and costs. Moreover, due to TM_0, silicon thinning is ineffective [42]. The excitation of parasitic modes inside silicon is unfavorable for the following reasons.

First, the transmission behavior of the TMV interconnect is disturbed by frequency-depending transmission dips (see Fig. 9). To investigate this effect, a b-t-b simulation was created without the M1 shield below the catchpad and the transmission behavior was observed when changing the silicon geometries width w_{si}, length l_{si}, and height t_{si}, as shown in the inset of Fig. 9. In this study, lateral dimensions, w_{si} and l_{si} were varied between 300 μm and 1500 μm, and the silicon thickness t_{si} between 100 μm and 300 μm. The transmission behaviors of four arbitrary resulting geometry variants of the underlying investigation are shown in Fig. 9. The transmission locally decreases due to the excitation of parasitic modes in silicon, depending on the actual silicon geometry. Thus, a part of the transferred power is lost. Moreover, the transmission dips depend on the lateral (w_{si}, l_{si}) and vertical (t_{si}) silicon geometry and on the relative localization of the TMV signal transition on the total chip area. If one of these geometries changes, the transmission magnitude $|s_{21}|$ also varies. Therefore, a robust transition without dependency on the silicon geometry and dimension cannot be guaranteed, but it would vary from application to application. Furthermore, during the assembly of the IC to the carrier board, the lateral rise of the conductive adhesive at the substrate edge would change the oscillation properties in the silicon. The lateral boundary will partially change from a dielectric condition to a conductive condition. This will influence the oscillation of parasitic modes in the silicon. As a result, the transmission properties will vary from sample to sample, and therefore, a stable condition cannot be guaranteed.

Second, mutual coupling between adjacent structures (e.g., antenna elements or transmission lines) occurs through silicon due to oscillating parasitic modes. This phenomenon is illustrated in the top view of the cross-section with two b-t-b TMV interconnects on one silicon bare die in Fig. 10. The oscillation of parasitic modes inside the silicon due to the excitation of transmission structure 1 is clearly visible. Moreover, the parasitic coupling of signal into transmission structure 2 is apparent. Depending on the silicon dimension, various minima and maxima of the electrical field occur, and the parasitic coupling between the two structures varies (see Fig. 11). Especially for antenna array designs with an element spacing of $\lambda_0/2$, strong coupling through silicon will arise. Therefore, no robust interconnect design is possible without silicon

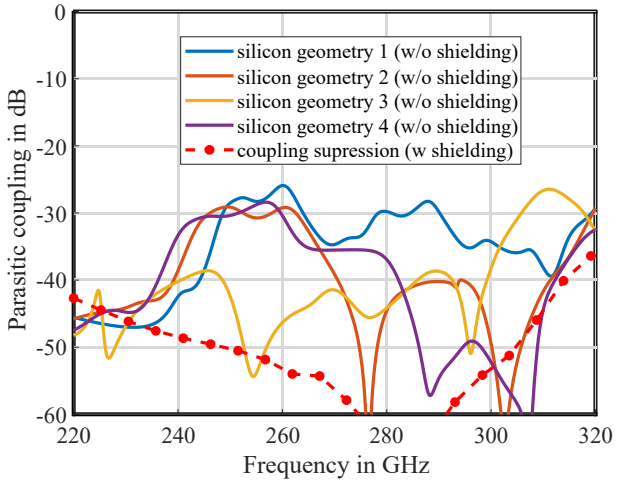

Fig. 11. Silicon geometry depended mutual coupling due to excitation of box modes inside silicon (w/o M1 shield) and significant suppression of mutual coupling (with M1 shield). Geometry definition see inset in Fig. 9.

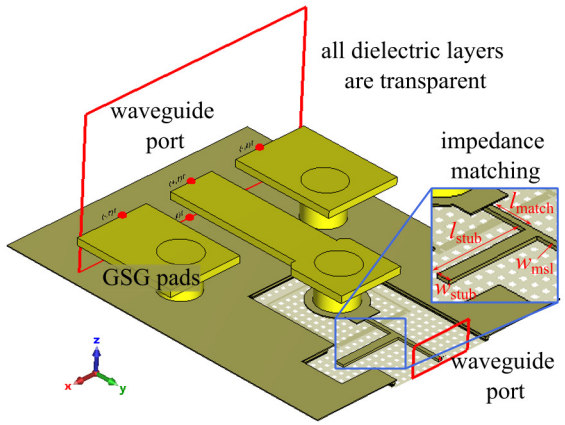

Fig. 12. TMV interconnect with impedance matching circuit in BEOL.

shielding. The mutual coupling between adjacent package transitions can be significantly suppressed to below $-40\,\mathrm{dB}$ by introducing a metal grid on metal M1 underneath the catchpad (see Fig. 11).

Third, the parasitic modes will partially radiate at the lateral boundary from silicon to air, resulting in an unwanted parasitic side radiation. This phenomenon is also visible on the right and on upper side in Fig. 10. The parasitic side radiation will interfere with the main radiators in the RDL layer and will cause unwanted antenna-pattern distortions [44]. Moreover, nearby IC components in heterogeneous system architectures can also be disturbed by unwanted parasitic chip-to-chip coupling.

In summary, the described phenomena do not represent robust conditions for the design of the TMV interconnect. The aim of this work is to develop a TMV interconnect with minimum parasitic radiation and, most importantly, with a signal transmission that is independent of the silicon geometry and the position of the structure in the chip area. Therefore, a metal grid on M1 was applied below the catchpad. The metal grid was applied due to DRC reasons (see Fig. 7). The openings in the metal grid are much smaller than $\lambda_{\mathrm{guided}}/100$ at $300\,\mathrm{GHz}$, so neither electrical field can be transmitted in silicon, nor the losses due to the grid structuring increase. The silicon shield was realized in M1 instead of M4 to increase the distance between catchpad and GND layer in order to minimize the parasitic capacitance C_{catchpad} (see Fig. 7). The penetration depth of the EM field due to the skin effect is less than $0.16\,\mu\mathrm{m}$ beyond $260\,\mathrm{GHz}$ due to the conductivity of M1. The metal M1 is thicker than the skin depth. The EM field decreases exponentially in metal and is attenuated to such an extent that there are no significant EM field components below M1. As a result, silicon is almost completely shielded from BEOL structures by the M1 shield and no parasitic mode resonance excitation occurs within silicon. The optimized matching of the TMV interconnect will be described in detail in the following subsection.

B. Optimization of Impedance-Controlled TMV Matching

Due to the silicon shielding with a metal grid in M1, as described in detail in section IV-A, a capacitance C_{catchpad} between the catchpad (AlPad) and the metal M1 layer occurs, and, thus, the arising impedance mismatch due to C_{catchpad} has to be compensated for. The simulation model of the single-ended TMV interconnect is shown in Fig. 12. Both the Ground-Signal-Ground (GSG) pads in RDL and the MSL with signal on M6 and GND on M4 are stimulated by waveguide ports within the frequency domain solver in CST Microwave Studio [45]. The C_{catchpad} is compensated for by a matching stub on M6 with GND on M4. The optimization goal of the impedance matching involves a trade-off between the following three requirements.

First, the matching circuit should be very compact, resulting in a low chip area consumption. Second, the matching should be broadband enough to provide sufficient bandwidth for wideband system applications. Third, the insertion loss and the parasitic radiation of the interconnect itself should be as low as possible for efficient power transfer into the package. Due

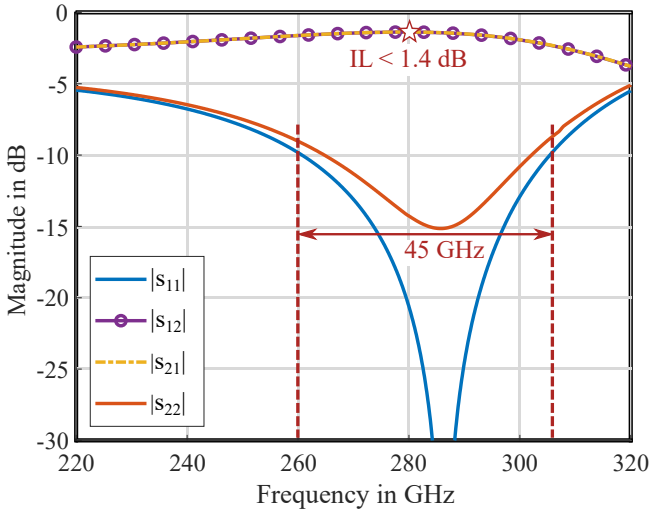

Fig. 13. Simulated S-parameters of the single ended TMV interconnect.

TABLE I
DIMENSIONS OF BEOL TRANSMISSION ELEMENTS.

parameter	w_{msl}	l_{match}	w_{stub}	l_{stub}	$d_{catchpad}$
dimension	5 µm	34.5 µm	10.6 µm	80 µm	60 µm

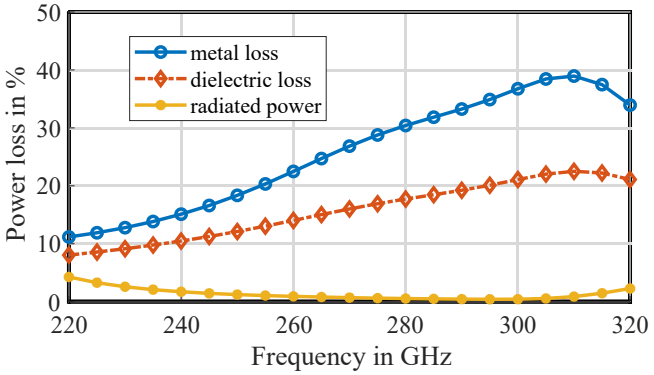

Fig. 14. Power dissipation over frequency. Parasitic radiation of the proposed TMV interconnect is negligible compared to metal and dielectric losses.

to its compactness, a matching stub was utilized to achieve an impedance-controlled signal transition. The frequency range in simulation is from 220 GHz to 325 GHz, which corresponds to the waveguide band WR03. The center frequency is 280 GHz to ensure sufficient measurement bandwidth for characterization in both directions in the upper half of the WR03 frequency band. The single ended scattering parameters of the optimized TMV are shown in Fig. 13. The return loss is above 10 dB from 260 GHz to 305 GHz resulting in a matching bandwidth of 45 GHz, which is sufficient for broadband sensing and

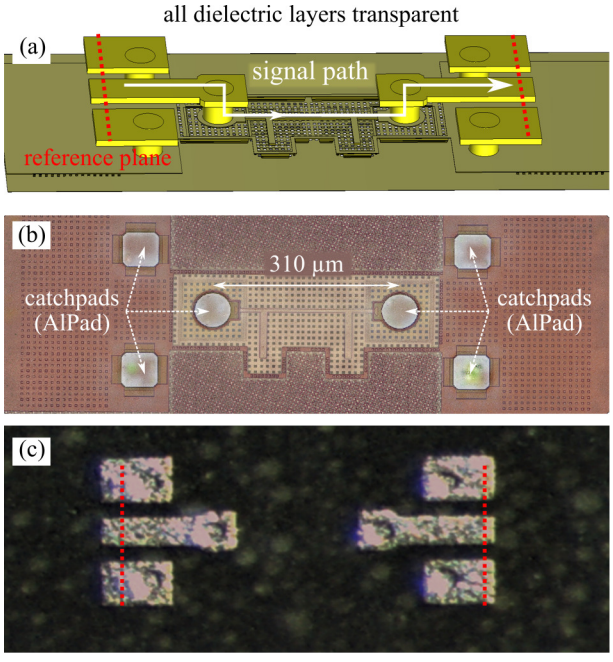

Fig. 15. (a) B-t-b simulation model. (b) Microscope image of the bare die BEOL with pads for TMV pillars. (c) Packaged IC with GSG pads in RDL.

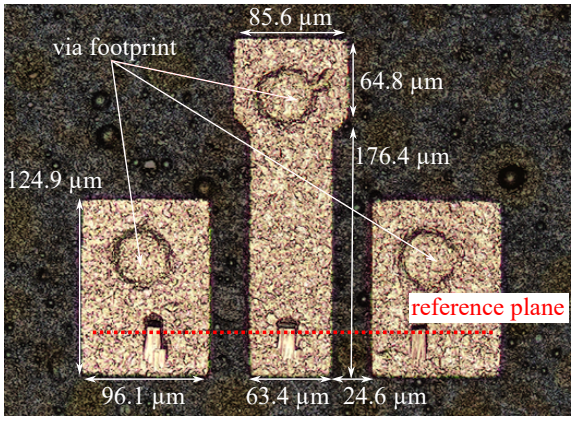

Fig. 16. Microscope image of the RDL GSG pads with measured dimensions.

communication applications. An insertion loss of lower than 1.4 dB indicates an efficient signal transition from BEOL to RDL.

C. Study of Parasitic Radiation

A major part of the optimization was an analysis of the parasitic radiation of the TMV interconnect. Therefore, a b-t-b simulation setup identical to the later manufactured structure was analyzed. In Fig. 14, the power loss profile of metallic and and parasitic radiation of the b-t-b model is plotted. The metallic loss is the main loss phenomenon due to skin effect and the finite conductivity. The dielectric loss is relevant with a maximum of 22 % beyond 300 GHz. The parasitic radiated power is below 2.5 % over the entire frequency band of interest and, therefore, negligible compared to the other losses. Consequently, the proposed interconnect enables an efficient, impedance-controlled signal transition without parasitic distortions or radiation. The b-t-b simulation model, the manufactured bare die, and the packaged assembly is shown in Fig. 15. The reference plane in the simulation setup is signified by the dotted line (Fig. 15(a)). The signal path of the b-t-b setup for simulation and measurement setup is highlighted. In Fig. 15(b) the microstrip transmission line in BEOL and the passivation opening for processing the TMV pillars are visible on the bare die. In Fig. 15(c), the packaged IC with the RDL GSG pads is shown. The TMV interconnects in the b-t-b setup are spaced sufficiently far apart for less coupling between the GSG probes during the measurement and for actual measurable transmission characterization from RDL to BEOL.

D. Structuring of the Redistribution Layer

To characterize the proposed TMV interconnect, transmission lines and GSG pads are designed in RDL. The GSG pads, especially the GND pads, have to be designed small and compact to prevent excitation of parasitic resonances in the GSG pads [43]. The manufactured RDL structures with the measured geometries can be seen in Fig. 16. A 50 Ω coplanar waveguide (CPW) interface is realized to keep the insertion loss at the RF probe scratch low and, thus, to keep

the measurement sensitivity high. The dimensions of the signal pad and the gap to the GND pads is a compromise between electrical performance and processability within the package assembly. Moreover, the reference plane after calibration (see details in Section V), the via footprint, and the scratch marks are illustrated in Fig. 16.

V. MEASUREMENT CHARACTERIZATION OF THE FAN-IN TMV INTERCONNECT

A. Measurement Setup

The TMV interconnect was characterized in the frequency band from 220 GHz to 325 GHz with a PNA-X vector network analyzer (VNA) and frequency extenders (R&S ZVA-Z325). The packaged assembly was contacted with Infinity GSG probes (WR03). Due to space constraints, a calibration kit could not be included on the packaged IC. Therefore, the measurement setup was calibrated with a TRL calibration on an impedance standard substrate (ISS 138-357). After the calibration, the measurement reference plane is located on the RF probe tip (see Fig. 16). The measurement setup, including the network analyzer, the frequency extenders, the GSG probes, and the wafer prober with the microscope is illustrated in Fig. 17.

B. Measurement Characterization of the Interconnect

The comparison of the initial simulated and measured reflection magnitudes of the b-t-b signal transition is shown in Fig. 18. A frequency shift of 15.3 GHz occurs between the center frequency of simulation and measurement, which corresponds to a relative deviation of 5.3 %. A similar frequency deviation is observable in the comparison of simulated and measured transmission magnitude in Fig. 19, wherein the maximal transmission (see red ellipses) is at 275 GHz in measurement and around 292 GHz in simulation. This results in a relative deviation of 6.2 %. Moreover, the transmission response over frequency differs between simulation and measurement. Furthermore, losses were not captured accurately

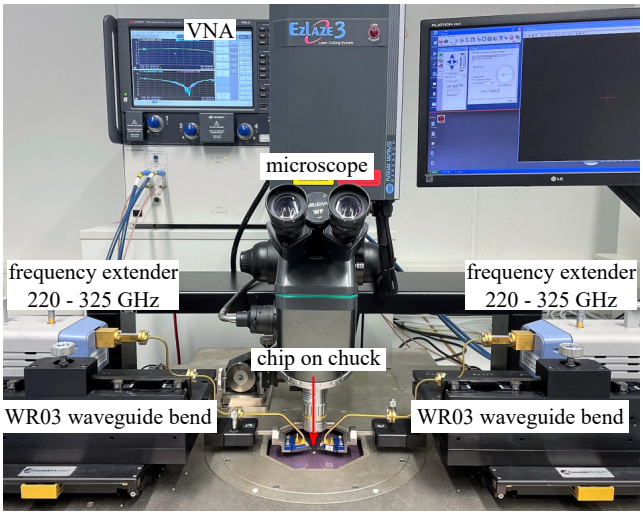

Fig. 17. On-wafer measurement setup for TMV interconnect characterization.

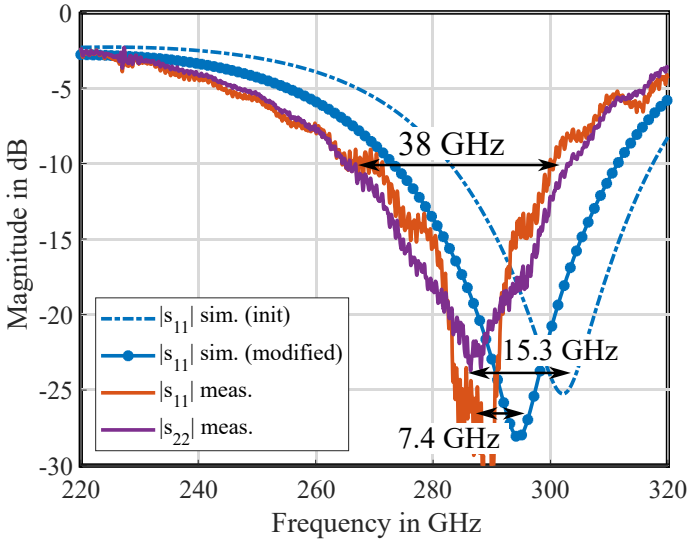

Fig. 18. Comparison of the measured reflection magnitude of the b-t-b assembly with the initial and adjusted simulation model (including the laser scanning microscope results).

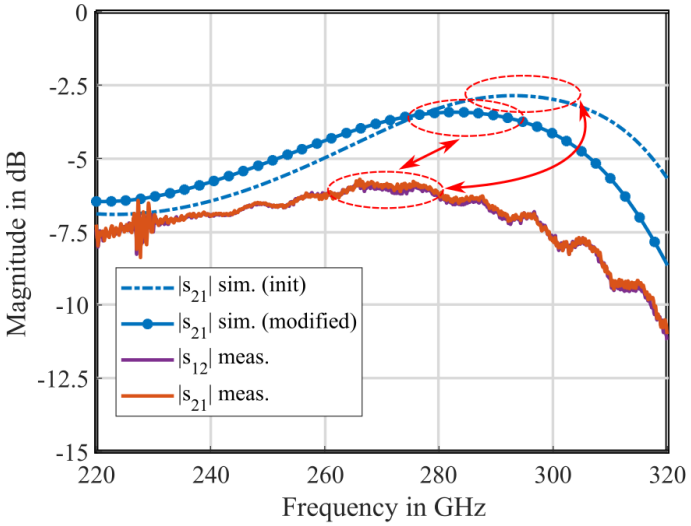

Fig. 19. Comparison of the measured transmission magnitude of the b-t-b assembly with the initial and adjusted simulation model (including the laser scanning microscope results).

enough in the simulation, resulting in a difference of 3 dB between the maxima of simulation and measurement. Regardless of the differences between simulation and measurement, the overall systems's functionality is well proven with the present results. However, further analysis is required to investigate the impacts and variances between both results, which is discussed in detail in the following subsection.

C. Optical and Electrical Examination of the Package

For a deeper comprehension of the differences between simulation and measurement results, different effects were investigated. The RDL geometries, the arrangement of TMV to RDL structures, the MC thickness and the dielectric properties of the MC were studied in detail. The height profile measurement of the packaged samples with respect to man-

ufacturing variations were measured with a laser scanning microscope from Keyence. The dimensions, such as widths, lengths, gaps and the metal heights of the RDL structures were inspected. Moreover, the surface roughness was considered. The measured average arithmetic of the RDL structures is $(0.203 \pm 0.025)\mu\mathrm{m}$. The dielectric properties of the MC have a crucial impact on the design of the TMV signal transition and on other in-package components, such as filters and antennas. Therefore, the used MC material was analyzed in detail in [46], [47] by a waveguide-based material characterization techniques. With this technique, the relative permittivity ε_r and the dielectric loss tangent $\tan(\delta)$ can be extracted directly in the frequency band of interest around $300\,\mathrm{GHz}$. In this study an ε_r = 3.51 and $\tan(\delta)$ = 0.0083 for frequencies close to $300\,\mathrm{GHz}$ were extracted and included in the modified re-simulation (see Section V-D).

Another main contributor to the occurring deviation between measurement and simulation result is the thickness of the MC, which defines the separation of RDL and BEOL. The thickness measurement t_MC was carried out at the cross-section of the packaged sample (see Fig. 6). In the assembly process, an MC thickness of 34-36 µm instead of the specified $40\,\mu\mathrm{m}$ was achieved. The results of the optical inspection, such as measured RDL geometries, surface roughness, metallization, MC thickness, and MC dielectric properties are considered in the modified simulation model. The most critical parameters for the initial and modified simulation are summarized in Tab. II.

D. Comparison of Results with Modified Simulation Model

The reflection magnitudes of the modified simulation and measurement are in high agreement with a center frequency offset of $7.4\,\mathrm{GHz}$, which corresponds to a relative deviation of less than $2.6\,\%$ (see Fig. 18). Moreover, the measured $10\,\mathrm{dB}$ matching bandwidth of the b-t-b transition is $38\,\mathrm{GHz}$, which is in high agreement with the simulation, and broadband enough for wideband SiP applications [12]. In Fig. 19, the transmission magnitude of the re-simulation and measurement is shown. The frequency-dependent transmission characteristics of simulation and measurement are in better agreement than in the initial comparison. The maximum in transmission of the modified simulation is around $285\,\mathrm{GHz}$, which minimizes the initial frequency deviation to $3.6\,\%$. Moreover, by appropriately modeling the dielectric losses in the simulation through the performed MC characterization, the differences between maximum levels of measured and simulated insertion losses could be reduced to less than $2.4\,\mathrm{dB}$. The minimum measured insertion loss of the b-t-b assembly is $5.7\,\mathrm{dB}$ at frequencies around $275\,\mathrm{GHz}$. In the frequency range from $245\,\mathrm{GHz}$ to $290\,\mathrm{GHz}$ the transmission coefficient drops by $1\,\mathrm{dB}$ compared to the measured maximum. This enables an efficient ultra-broadband signal transition from package to IC and vice versa over a bandwidth of $45\,\mathrm{GHz}$. The measurement includes the losses of two TMV interconnects, and the losses of the MSL between both interconnects within the b-t-b assembly (see Fig. 15). Thus, the single TMV interconnect has a minimal insertion loss below $2.8\,\mathrm{dB}$ at $275\,\mathrm{GHz}$. The current research involves the characterization of microstrip line MSL losses in the BEOL at frequencies beyond $220\,\mathrm{GHz}$ in order to de-embed the insertion loss of MSLs in future measurements.

TABLE II
COMPARISON OF INITIAL AND MODIFIED SIMULATION PARAMETERS.

Parameter	t_MC	$\varepsilon_\mathrm{r,\,MC}$	$\tan(\delta)_\mathrm{MC}$	$R_\mathrm{q,\,rms,\,RDL}$
Initial dimension	40 µm	3	0.005	0 µm
Modified dimension	34 µm	3.51	0.0083	0.203 µm

By re-simulating the setup using the actual assembly dimensions and heights obtained by laser scanning and considering the results of the material characterization, the initial differences between simulation and measurement were significantly reduced. This good correspondence strengthens the proof of functionality of the TMV interconnect functionality. Furthermore, it is shown that it is feasible to capture process deviations and to accurately model them in the simulation setup. This enables the identification of critical performance parameters (e.g., MC thickness) for targeted optimization in further production cycles.

VI. CONCLUSION AND OUTLOOK

This paper presents a TMV interconnect from BEOL to fan-in WLB package with measured matching bandwidth of $38\,\mathrm{GHz}$ and a measured de-embedded insertion loss of less than $2.8\,\mathrm{dB}$ per TMV interconnect at $275\,\mathrm{GHz}$. Compared to other SiP assemblies, this work uses a fan-in instead of a fan-out WLB, which enables vertical rather than lateral integration of passive package structures on top of BEOL. The compact connection of active and passive components results in a smaller form factor for the entire SiP, lower insertion loss per interconnection, and improved overall system performance. The proposed TMV interconnect is independent of wafer geometries, such as thickness, width, and length, and has minimal parasitic radiation at the interconnect transition. The high agreement of simulation and measurement verifies the functionality of this robust and impedance-controlled TMV interconnect for future broadband communication and sensing SiP applications and enables also chip-to-chip interconnections for 3D heterogeneous system design.

In future work, the copper pillar diameter could be further reduced, to achieve a more compact catchpad, lower capacity, and, thus, to minimize the insertion loss of the interconnect. Moreover, by further minimizing the TMV dimensions, the impedance matching bandwidth would be increased. In addition, silicon LBE could be used underneath the catchpad to reduce the capacity of the catchpad, although the manufacturing complexity will increase.

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REFERENCES

[1] J. Al-Eryani, H. Knapp, J. Kammerer, K. Aufinger, H. Li, and L. Maurer, "Fully Integrated Single-Chip 305–375-GHz Transceiver With On-Chip Antennas in SiGe BiCMOS," *IEEE Trans. on Terahertz Sci. and Technol.*, vol. 8, no. 3, pp. 329–339, 2018.

[2] M. Furqan, F. Ahmed, and A. Stelzer, "A SiGe 122-GHz FMCW Radar Sensor with 21.5 dBm EIRP based on a 43-Element Antenna Array in an eWLB Package," in *IEEE MTT-S Int. Conf. Microw. Intel. Mob. (ICMIM)*, 2018, pp. 1–4.

[3] R. Hasan, M. H. Eissa, W. A. Ahmad, H. J. Ng, and D. Kissinger, "Wideband and Efficient 256-GHz Subharmonic- Based FMCW Radar Transceiver in 130-nm SiGe BiCMOS Technology," *IEEE Trans. Microw. Theory and Techn.*, vol. 71, no. 1, pp. 59–70, 2023.

[4] M. Jenning, B. Klein, R. Hahnel, and D. Plettemeier, "On-Chip Integrated Antennas for 200 GHz Applications," in *IEEE Int. Conf. Ubiquitous Wirel. Broadband (ICUWB)*, 2015, pp. 1–5.

[5] R. Hahnel, B. Klein, C. Hammerschmidt, D. Plettemeier, P. V. Testa, C. Carta, and F. Ellinger, "Distributed on-chip antennas to increase system bandwidth at 180 GHz," in *Ger. Microw. Conf. (GeMiC)*, 2016, pp. 161–164.

[6] J. Grzyb, P. Rodríguez-Vázquez, S. Malz, M. Andree, and U. R. Pfeiffer, "A SiGe HBT 215–240 GHz DCA IQ TX/RX Chipset With Built-In Test of USB/LSB RF Asymmetry for 100+ Gb/s Data Rates," *IEEE Trans. Microw. Theory Techn.*, vol. 70, no. 3, pp. 1696–1714, 2022.

[7] D. Kissinger, "D-Band and Terahertz Frontends for 6G Wireless Communications in SiGe BiCMOS Technologies," in *IEEE MTT-S Int. Wirel. Symp. (IWS)*, vol. 1, 2022, pp. 1–3.

[8] M. Pauli, B. Göttel, S. Scherr, A. Bhutani, S. Ayhan, W. Winkler, and T. Zwick, "Miniaturized Millimeter-Wave Radar Sensor for High-Accuracy Applications," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 5, pp. 1707–1715, 2017.

[9] M. Frank, T. Reissland, F. Lurz, M. Voelkel, F. Lambrecht, S. Kiefl, P. Ghesquiere, H. Jalli Ng, D. Kissinger, R. Weigel, and A. Koelpin, "Antenna and Package Design for 61- and 122-GHz Radar Sensors in Embedded Wafer-Level Ball Grid Array Technology," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 12, pp. 5156–5168, 2018.

[10] T. Merkle, D. Meier, S. Wagner, A. Tessmann, M. Kuri, H. Massler, and A. Leuther, "Broadband 240-GHz Radar for Non-Destructive Testing of Composite Materials," *IEEE J. Solid-State Circuits*, vol. 54, no. 9, pp. 2388–2401, 2019.

[11] D. Kissinger, M. Kaynak, and A. Mai, "Integrated Millimeter-Wave and Terahertz Analyzers for Biomedical Applications," *IEEE Trans. Microw. Theory Techn.*, vol. 70, no. 11, pp. 5141–5158, 2022.

[12] V. Petrov, T. Kurner, and I. Hosako, "IEEE 802.15.3d: First Standardization Efforts for Sub-Terahertz Band Communications toward 6G," *IEEE Communications Magazine*, vol. 58, no. 11, pp. 28–33, 2020.

[13] V. Issakov, M. Wojnowski, H. Knapp, S. Trotta, H.-P. Forstner, K. Pressel, and A. Hagelauer, "Co-simulation and co-design of chip-package-board interfaces in highly-integrated RF systems," in *IEEE Bipolar/BiCMOS Circuits Techn. (BCTM)*, 2016, pp. 94–101.

[14] V. Lammert, M. Hamouda, R. Weigel, and V. Issakov, "A 122 GHz On-Chip 3-Element Patch Antenna Array with 10 GHz Bandwidth," in *Europ. Microw. Conf. (EuMC)*, 2021, pp. 599–602.

[15] T. Pfahler, M. Vossiek, and J. Schür, "Compact and Broadband 300 GHz Three-Element on-chip Patch Antenna," in *IEEE Radio and Wirel. Symp.*, 2023, pp. 139–142.

[16] B. Goettel, W. Winkler, A. Bhutani, F. Boes, M. Pauli, and T. Zwick, "Packaging Solution for a Millimeter-Wave System-on-Chip Radar," *IEEE Trans. Compon., Packag. and Manuf. Technol.*, vol. 8, no. 1, pp. 73–81, 2018.

[17] C. C. Liu, S.-M. Chen, F.-W. Kuo, H.-N. Chen, E.-H. Yeh, and C.-C. e. a. Hsieh, "High-performance integrated fan-out wafer level packaging (InFO-WLP): Technology and system integration," in *Int. Electron Devi. Meeting*, 2012, pp. 14.1.1–14.1.4.

[18] M. Kawano, "Technology Trends in 2.5D/3D Packaging and Heterogeneous Integration," in *5th IEEE Electron Devices Technol. and Manuf. Conf. (EDTM)*, 2021, pp. 1–3.

[19] E. Seler, M. Wojnowski, W. Hartner, J. Böck, R. Lachner, R. Weigel, and A. Hagelauer, "3D rectangular waveguide integrated in embedded Wafer Level Ball Grid Array (eWLB) package," in *IEEE 64th Electr. Compon. Technol. Conf. (ECTC)*, 2014, pp. 956–962.

[20] H. Theuss, C. Geissler, and W. Hartner, "Trends in Fan Out Wafer Level Packaging," in *13th International Conf. Advan. Semicond. Devices Microsys. (ASDAM)*, 2020, pp. 106–110.

[21] M. Wojnowski, R. Lachner, J. Böck, C. Wagner, F. Starzer, G. Sommer, K. Pressel, and R. Weigel, "Embedded wafer level ball grid array (eWLB) technology for millimeter-wave applications," in *IEEE 13th Electr. Packag. Technol. Conf.*, 2011, pp. 423–429.

[22] T. Meyer, K. Pressel, G. Ofner, and B. Römer, "System integration with eWLB," in *Electr. Sys. Integration Technol. Conf.*, 2010, pp. 1–9.

[23] K. Pressel, G. Beer, T. Meyer, M. Wojnowski, M. Fink, G. Ofner, and B. Römer, "Embedded wafer level ball grid array (eWLB) technology for system integration," in *IEEE CPMT Symposium Japan*, 2010, pp. 1–4.

[24] X. Gu, D. Liu, and B. Sadhu, "Packaging and Antenna Integration for Silicon-Based Millimeter-Wave Phased Arrays: 5G and Beyond," *IEEE J. Microw.*, vol. 1, no. 1, pp. 123–134, 2021.

[25] A. O. Watanabe, M. Ali, S. Y. B. Sayeed, R. R. Tummala, and M. R. Pulugurtha, "A review of 5g front-end systems package integration," *IEEE Trans. Compon., Packag. and Manuf. Technol.*, vol. 11, no. 1, pp. 118–133, 2021.

[26] M. Brunnbauer, E. Fürgut, G. Beer, and T. Meyer, "Embedded wafer level ball grid array (eWLB)," in *Electr. Packag. Technol. Conf.*, 2006, pp. 1–5.

[27] C.-H. Tsai, J.-S. Hsieh, M. Liu, E.-H. Yeh, H.-H. Chen, C.-W. Hsiao, C.-S. Chen, C.-S. Liu, M.-J. Lii, C.-T. Wang, and D. Yu, "Array antenna integrated fan-out wafer level packaging (InFO-WLP) for millimeter wave system applications," in *IEEE Intern. Electron Dev. Meeting*, 2013, pp. 25.1.1–25.1.4.

[28] C.-T. Wang, T.-C. Tang, C.-W. Lin, C.-W. Hsu, J.-S. Hsieh, C.-H. Tsai, K.-C. Wu, H.-P. Pu, and D. Yu, "InFO-AiP Technology for High Performance and Compact 5G Millimeter Wave System Integration," in *IEEE 68th Electr. Compon. Technol. Conf. (ECTC)*, 2018, pp. 202–207.

[29] M. Wojnowski, M. Engl, M. Brunnbauer, K. Pressel, G. Sommer, and R. Weigel, "High Frequency Characterization of Thin-Film Redistribution Layers for Embedded Wafer Level BGA," in *9th Electr. Packag. Technol. Conf.*, 2007, pp. 308–314.

[30] S. Beer, H. Gulan, M. Pauli, C. Rusch, G. Kunkel, and T. Zwick, "122-GHz chip-to-antenna wire bond interconnect with high repeatability," in *IEEE MTT-S Int. Microw. Symp. Dig.*, 2012, pp. 1–3.

[31] S. Beer, C. Rusch, H. Gulan, B. Göttel, M. G. Girma, J. Hasch, W. Winkler, W. Debski, and T. Zwick, "An Integrated 122-GHz Antenna Array With Wire Bond Compensation for SMT Radar Sensors," *IEEE Trans. Ant. Propag.*, vol. 61, no. 12, pp. 5976–5983, 2013.

[32] A. Bhutani, B. Göttel, A. Lipp, and T. Zwick, "Packaging Solution Based on Low-Temperature Cofired Ceramic Technology for Frequencies Beyond 100 GHz," *IEEE Trans. Compon., Packag. and Manuf. Technol.*, vol. 9, no. 5, pp. 945–954, 2019.

[33] A. Bhutani, B. Goettel, M. Pauli, and T. Zwick, "122 GHz FMCW Radar System-in-Package in LTCC Technology," in *49th Europ. Microw. Conf. (EuMC)*, 2019, pp. 1008–1011.

[34] M. PourMousavi, M. Wojnowski, R. Agethen, R. Weigel, and A. Hagelauer, "The impact of embedded wafer level BGA package on the antenna performance," in *IEEE APS Topical Confe. Ant. Propag. Wirel. Com. (APWC)*, 2013, pp. 828–831.

[35] F. Ahmed, M. Furqan, and A. Stelzer, "120-GHz and 240-GHz Broadband Bow-Tie Antennas in eWLB Package for High Resolution Radar Applications," in *48th European Microwave Conference (EuMC)*, 2018, pp. 1109–1112.

[36] E. Bekker, A. Bhutani, L. G. de Oliveira, T. Antes, and T. Zwick, "Broadband Split Ring Resonator-Based Antennas at 140 GHz in Embedded Wafer Level Ball Grid Array Technology," in *Int. Workshop Ant. Technol.*, 2022, pp. 60–63.

[37] M. PourMousavi, M. Wojnowski, K. Pressel, G. Sommer, and R. Weigel, "Passive components using quasi-CPW in eWLB package," in *19th Int. Conf. Microw. Radar Wirel. Com.*, vol. 2, 2012, pp. 709–712.

[38] A. Bhutani, E. Bekker, L. G. de Oliveira, M. Pauli, and T. Zwick, "140 GHz Broadband Antenna in Embedded Wafer-Level Ball Grid Array Technology," in *15th Europ. Conf. Ant. Propag.*, 2021, pp. 1–5.

[39] M. Furqan, F. Ahmed, R. Feger, K. Aufinger, and A. Stelzer, "A 122-GHz system-in-package radar sensor with BPSK modulator in a 130-nm SiGe BiCMOS technology," in *46th Europ. Microw. Conf. (EuMC)*, 2016, pp. 683–686.

[40] M. Wojnowski, G. Sommer, K. Pressel, and G. Beer, "3D eWLB — Horizontal and vertical interconnects for integration of passive components," in *IEEE 63rd Electr. Compon. Technol. Conf.*, 2013, pp. 2121–2125.

[41] C. Balanis, *Antenna Theory, Analysis and Design*, N. Y. Wiley-Interscience, Ed. New York: Wiley-Interscience, 2005.
[42] D. M. Pozar, *Microwave engineering; 4rd ed.* Hoboken, NJ: Wiley, 2011.
[43] D. Müller, J. Schäfer, H. Massler, M. Ohlrogge, T. Zwick, and I. Kallfass, "Impact of Ground Via Placement in On-Wafer Contact Pad Design up to 325 GHz," *IEEE Trans. Compon., Packag. and Manuf. Technol.*, vol. 8, no. 8, pp. 1440–1450, 2018.
[44] V. Lammert, M. Leyrer, M. Hamouda, R. Weigel, and V. Issakov, "Dual-Mode Substrate Wave Cancellation in a 120 GHz 2 × 2 On-Chip Dipole Array," *IEEE Trans. Ant. Propag.*, vol. 70, no. 8, pp. 6683–6691, 2022.
[45] "Cst studio suite," 2021. [Online]. Available: http://www.3ds.com
[46] T. Pfahler, G. Gold, K. Lomakin, L. Engel, J. Schür, and M. Vossiek, "Ultra-Wideband Complex Permittivity Extraction of IC Packaging Materials beyond 100 GHz," in *IEEE MTT-S Int. Microw. Symp. Dig.*, 2021, pp. 345–348.
[47] T. Pfahler, G. Gold, F. Bachbauer, J. Schür, and M. Vossiek, "Complex Permittivity Extraction of IC-Package Materials beyond 110 GHz by Band-Limited Waveguide-Cavity Measurements," in *53rd Europ. Microw. Conf. (EuMC)*, 2023, pp. 568–571.

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