



The first stage is formed using the well-known CCDD because the NMOS has lower threshold. The body terminal of the PMOS is connected to either RF+ or RF- signal via coupling capacitors to control the threshold voltage during the ON and the OFF states.

The second and the consequent stages are designed using PMOS only and connected in a different way as shown in Figure 1. Hence an n-well process instead of the twin-well is used to fabricate these types of rectifiers. Consequently, less area and less cost will be the main achievement. In addition, the DC output increases almost linearly with the number of stages and can produce higher output voltage.

The rectifier operation is as follows: the first stage is normal CCDD, and during the negative half of the cycle, transistors MN1 and MP2 will be ON, and hence  $C_1$  will charge to  $V_a - V_{DS1}$  and the charge in  $C_2$  is pumped to the output. The opposite will happen in the positive half of the cycle. The same will happen for next PMOS stage where  $C_1$  will charge through MP3 and the charge in  $C_2$  will be pumped to the output via MP6

### III. SIMULATION RESULTS

The proposed design is implemented in  $0.18\mu\text{m}$  TSMC CMOS process technology and verified using Cadence Virtuoso environment. The aspect ratios of transistors are chosen for CCDD to be  $MN1=MN2=20\mu\text{m}/0.18\mu\text{m}$  and  $MP1=MP2=100\mu\text{m}/0.18\mu\text{m}$ . For the second and consequent stages the size for all transistors is  $20\mu\text{m}/0.18\mu\text{m}$ . The flying

capacitors  $C_1 = C_2 = C_b = 1\text{pF}$ , and  $C_L = 2\text{pF}$ . The frequency of the signal is  $920\text{MHz}$ .

The first two hybrid stage design was simulated for different loads namely ( $5\text{k}\Omega$ ,  $10\text{k}\Omega$ ,  $50\text{k}\Omega$ ). Plots of the DC output voltages are shown in figure 2. It is clear from the figure that increasing the load will increase the output voltage. However, it was noted that increasing the load beyond  $100\text{k}\Omega$  will not make a significant increase in the output voltage.

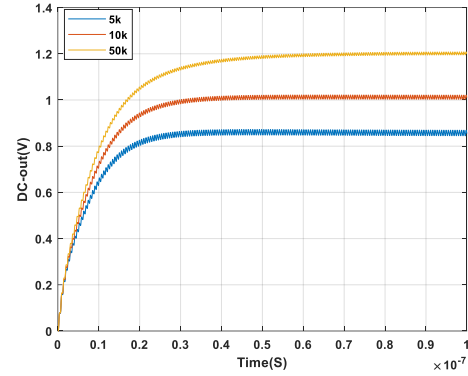


FIGURE 2. Plots of the DC output voltage for different loads.

To achieve a higher DC output voltage, one can cascade the stages without adding any capacitors between stages as shown in figure 3. Plot of the simulated DC output voltage as a function of the number of stages is shown in Figure 4. It is clear from the plot that DC output increases almost linearly with the number of stages. The DC output reaches  $8\text{V}$  when cascading 21 stage.

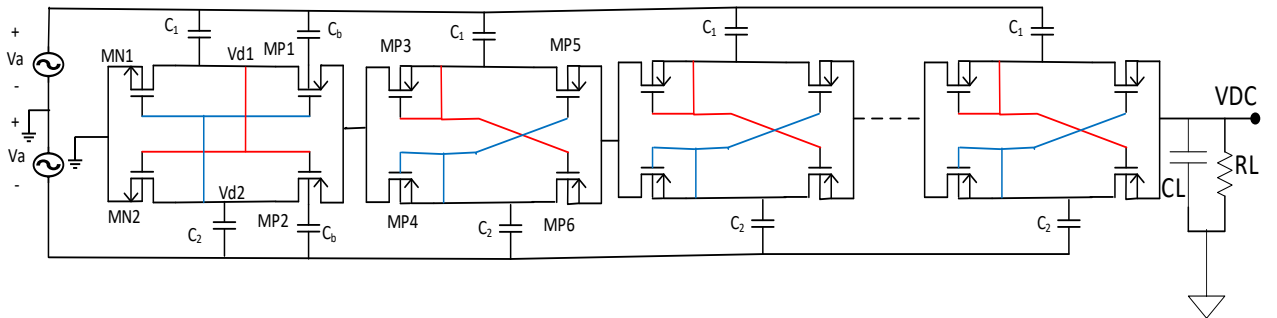


FIGURE 3. Connection for cascading stages

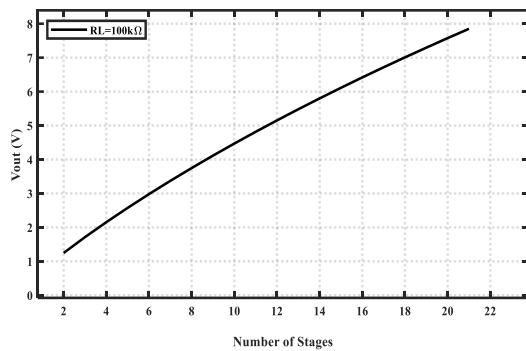


FIGURE 4. Plot of the output voltage vs the number of stages.

Plots of the efficiency of the rectifier for different loads are shown in figure 5. It can be seen that the PDR is 33dB.

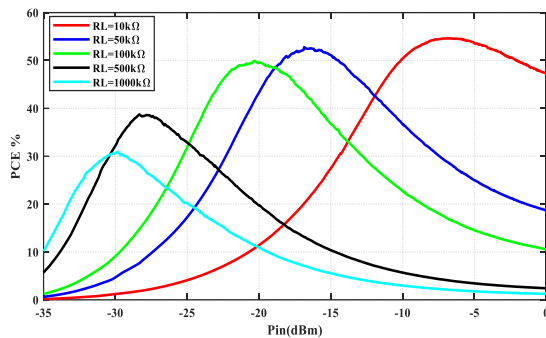


FIGURE 5. Plots of efficiency vs the input power for different loads.

#### IV. CONCLUSION

A new n-well process RF-DC converter is developed. The design uses CCDD as a first stage and the next stages are all designed using PMOS transistors. The proposed design provides a linear DC output voltage with the number of stages and achieves excellent input power range for PCE >20%. We believe that there is a chance to improve the efficiency and make this hybrid design the most efficient in all aspects.

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