A 98.5-dB DR Incremental ΔΣ ADC with Dynamic Zoom and Extended Counting for Audio Application

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Abstract

A three-step discrete-time incremental analog-to-digital converter (IADC) combines zoom, IΔΣM and dual-mode SAR-assisted extended counting (EC). The IADC reuses the SAR ADC to reduce hardware cost by reconfiguring its DAC array to either a 2-bit quantizer of the core IΔΣM or a 5-bit EC ADC. Clocked at 4MHz with an OSR=99, the proposed IADC achieves SNDR and DR of 93dB and 98.5dB, respectively, in a BW of 20.2kHz.

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Introduction: High-fidelity audio systems for smart home applications often require high precision ADCs with large dynamic range (DR) and high power efficiency. To achieve high accuracy, prior art ADCs usually employ oversampled delta-sigma modulators (ΔΣMs). However, conventional ΔΣMs are free running, and they suffer from idle tones that can be easily picked up by human ears. Incremental ΔΣMs (IΔΣMs) solve this issue by using simple filter structures with periodic reset. Although previous audio-band IΔΣMs achieve a DR of more than 100dB [1][2], they typically rely on large OSR (256-8192) at a high-frequency system clock (10-500MHz), respectively.

This letter presents a discrete-time (DT) incremental ΔΣM, it combines zoom and extended counting (EC) to reduce OSR and improve power efficiency. As a result, this hybrid IADC achieves state-of-the-art SNDR and DR 93 dB and 98.5 dB, respectively, in an audio bandwidth of 20.2 kHz with a moderate OSR of 99. The total power consumption is 430 μW from 1.8V supply.

Three-step IADC: Figure 1 illustrates the IADC topology. D_{out} combines the outputs of three sub-conversion results: 1) Zoom: 5-bit coarse digitization of the input signal by an asynchronous Zoom-SAR; 2) IΔΣM: 2-bit digital output of a 2^{nd}-order IΔΣM, 3) EC: 5-bit output by digitizing the loop filter residue where the SAR quantizer is reconfigured in 5-bit mode. The overall IΔΣM employs feedforward structure to achieve

flat unit signal-transfer function (STF), which can suppress the leakage of Zoom-SAR quantization errors [4].

Fig 1 *Block diagram of the proposed three-step IADC*

Circuit Implementation: Figure 2 shows the circuit and timing implementation. When RST1 is low, on the rising edge of $\mathbf{\Phi 1}$, Zoom-SAR digitizes the input signal, and the 2-bit quantizer digitizes the output V_{O3} of the feedforward amplifier (FF AMP) before the falling edge of $\mathbf{\Phi 2}$. When RST1 is high, the first-stage integrator resets, the second stage integrator acts as a hold amplifier to store the residue. The FF AMP then switches to integrator mode to integrate the residue, and finally integrates V_{O3} to approximately 8 times of V_{RES}. Next, the SAR quantizer is configured to a 5-bit mode to digitize the amplified V_{O3}. RST2 is set to high and the second stage integrator resets. Bootstrap switches are employed to linearize the input sampling.

In this work, the 2-bit quantizer output controls reference voltages (D_{ZOOM}+2)×LSB, (D_{ZOOM}+1)×LSB, D_{ZOOM}×LSB and (D_{ZOOM}-1)×LSB to provide a redundancy of 2 LSBs, where LSB is the quantization step of the Zoom-SAR, i.e. 112.5mV for a 3.6V full scale input.

Dual-mode SAR ADC: Figure 3 shows the implementation of the dual-mode SAR ADC. For simplicity, only a single-ended version is illustrated while the actual ADC is fully differential.

The 5-bit mode EC ADC is a 5-bit asynchronous SAR. The 2-bit mode SAR for quantizer is implemented by assigning the DACs into two segments, thus dividing the full scale into four segments. The dual-mode SAR not only realizes the desired quantizer threshold, but also implementing an extended count of 5 bits, resulting in hardware reuse and so saving the chip area.

Fig 2 *Circuit implementation of the Three-step IADC, during (a) phase 1 and (b) phases 2 and 3. (c) switching activities*

Fig 3 *Block diagram of proposed dual-mode asynchronous SAR*

Fig 4 *Die photomicrograph of the 180nm CMOS three-step IADC*

Measurement results: The ADC was manufactured in a standard 180nm CMOS process and occupies an active area of 0.432mm^2as shown in Fig. 4. The prototype consists of the IADC, auxiliary digital circuit, and bias generator. Chip measurements were performed by using a high precision audio source and a low noise off-chip regulator providing reference voltages of 1.8V and 0V.

Fig 5 *Output spectrum with DWA turned "off" and "on"*

Fig 6 *Dynamic range*

Fig.5 shows the measured spectrum with a -0.11dBFS input signal at 15kHz with the DWA "on" and "off." The SNDR increases from 80.7dB to 93dB when the DWA is enabled.

When using a 15kHz sinusoidal input signal, the measured SNR and SNDR versus input signal amplitude are shown in Figure. 6, where 0-dB FS corresponds to a differential input voltage of 3.6 V_{PP}. A peak SNDR of 93dB is achieved at full-scale input and this indicates a dynamic range (DR) of 98.5dB. This translates into a state-of-the-art Schreier FoM_{SNDR} of 169.7dB and a $FoM_{DR}$of 175.2dB.

Table I summarizes the performance of this IADC and its comparation with the state of the art. Thanks to the hybrid three-step conversion and reconfigurable SAR, this work achieves excellent SNDR and DR while working at a much lower oversampling ratio with less power consumption.

TABLE I

Conclusion: Combining IΔΣM, zoom, and extended counting while employing a dual-mode SAR, the proposed hybrid IADC significantly reduced the OSR and system clock thus achieving state-of-the-art perfor-

mance in DR and SNDR in the entire audio bandwidth with great power efficiency. This IADC provides new solutions for energy-efficient, high-fidelity audio systems.

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