A 64-Channel sub-1nC Charge-balanced Stimulator IC for Seizure Suppression

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Abstract

We present a 64-channel implantable neural stimulator with sub-nC charge balanced current stimulation for seizure suppression applications. The regulated cascode current driver achieves almost full VDD compliance voltage range. A passive charge balancing by shorting working and reference electrodes with a bootstrapped switch keeps the residual charge level within a safe limit, enabling faster-switching operation. The stimulation parameters, such as current pulse width, channel activation, activation frequency, and current amplitude, are highly reconfigurable and adjusted through the SPI interface. Significantly, the current amplitude can be varied from 1μA to 1.8 mA. As a result, the proposed neural stimulator fabricated with a 0.18μm standard CMOS process effectively suppresses seizures within a safe limit with a residual charge of less than 1nC through the in-vivo test.

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Introduction: Epilepsy is a brain disease in which paralysis of brain function occurs repeatedly due to transient over-excitation of brain nerve cells, which is the second most common chronic disease of the nervous system after headaches. Electrical brain stimulation is increasingly used in medication-resistant seizure therapy [1].

In the electrical current stimulator, once the bi-phasic current is injected from the working electrode to the reference electrode, the voltage level of the working electrode fluctuates according to the electrode and tissue impedance. Therefore, a high compliance voltage is required to deliver an applicable amount of charge to the tissue regardless of the amplitude of the stimulation current. Conventional current mode stimulator circuits exploit the high-voltage CMOS technology to achieve a high compliance voltage of the stimulator [2,3], which has significant disadvantages in power, area, and cost consumption.

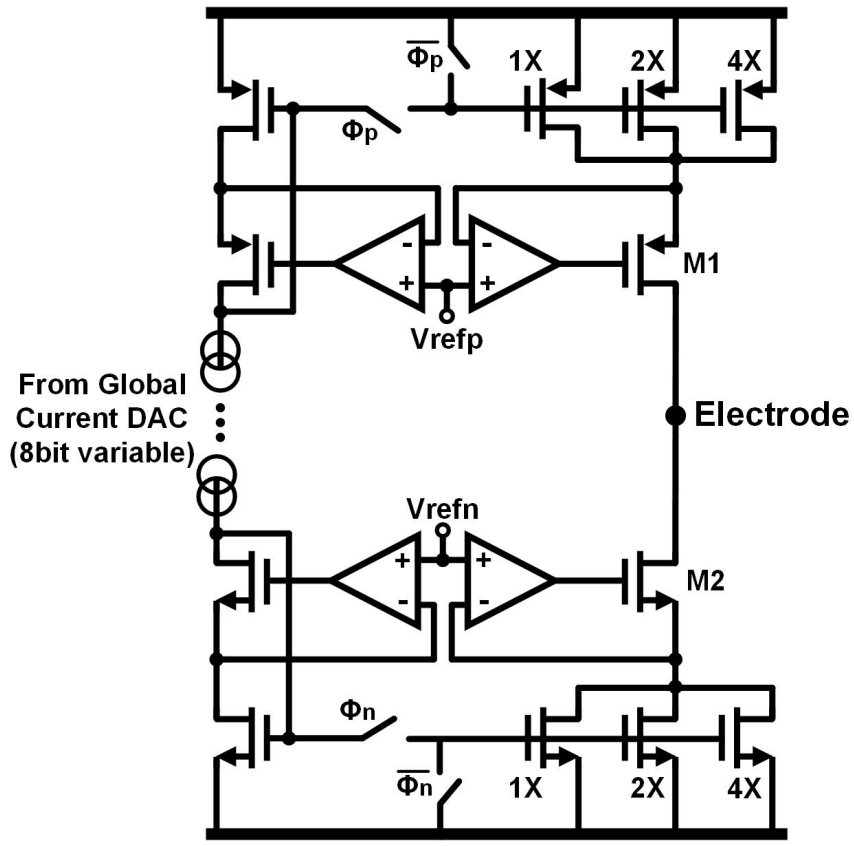
Since the injection of the stimulation current causes the accumulation of residual charge at the electrode-electrolyte interface, creating a DC current flow that damages nerve tissue and corrodes the electrodes,

the charge balancing function is required to mitigate the safety issue. While the active charge balancing (CB) scheme can remove the residual charge without an additional long discharging period, resulting in fast stimulation frequency, the passive CB scheme has advantages in terms of circuit complexity, power, and area consumption [2,3,4]. Given that the electrical stimulation for seizure suppression is effective in the low stimulation frequency of 5Hz [5], the passive CB scheme that minimizes the time constant associated with the resistance of the passive switches and the impedance of the electrode-tissue interface for reducing the discharge period can be a feasible alternative to the active CB scheme.

This work proposes a 64-channel neural stimulator integrated circuit (IC) for seizure suppression application. The compliance voltage is maximized by employing a regulated cascode output stage. Given that the safe range of residual charge, which prevents tissue damage and electrode corrosion is 15nC [6], we adopt a passive charge balancing scheme with a bootstrapped switch of low on-resistance. As a result, the proposed charge-balanced stimulator maintains the residual charge below 1nC within the safety limit at the stimulation frequency of 5Hz, with in-vivo verification of suppressing seizures in animal tests.

Proposed System Design: Fig. 1 shows the architecture of the proposed 64-channel neural stimulator system. The overall system consists of a global 8-bit current digital-to-analog converter (DAC), level shifter, bandgap reference, digital controller, and 64-channel stimulator units composed of the output current driver with local 3-bit DAC and bootstrapped switch for charge balancing as shown in Fig. 1a. The global 8-bit DAC and local 3-bit DAC can control stimulation current from 1μA up to 1.8mA. The output driver implemented with a regulated cascode current source generates bi-phasic pulses capable of stimulating tissue with an almost complete VDD (5V) compliance range by setting Vrefp and Vrefn to 4.98V and 0.02V, respectively. Stimulation current pulse is configured with sequence anodic/cathodic, off, cathodic/anodic, and discharge periods. The bootstrapped switch shorts the working electrodes to the reference electrode biased at the voltage of VCM with low on-resistance at the discharge period. The level shifter changes the DC level of the digital signal from the digital controller (1.8V) to the high voltage level for the output current driver (5V). A digital controller with an SPI slave interface operating in 10MHz configures the registers for controlling the stimulation parameters of CH (which channel is activated), Ton (timing information of anodic, off, cathodic, and discharge pulses), DAC (current of the global DAC), and Amp(current of the local DAC in stimulation unit). The output driver operates in a 5V supply voltage while the other is under the 1.8V supply voltage with standard CMOS technology. Fig. 1b shows stimulation pulses generated by the SPI interface, showing that the MOSI (master output slave input) command signal triggers the stimulation. All stimulation parameters are independently configurable, and the SPI commands can configure mono-phasic, symmetric, and asymmetric bi-phasic stimuli. The pulse width can be controlled from 1μs up to 1023μs.

Fig. 2 shows the schematic of the output current driver. The impedance of output node is boosted by a regulated cascode scheme for constant current injection, regardless of the voltage fluctuation across the electrode-tissue impedance with wide range of the current amplitude. The output compliance voltage is maximized through the negative feedback loop through the OTAs (operating transconductance amplifiers), ensuring the source node voltages of M1 and M2 are kept as constant as possible with Vrefp of 4.98V and Vrefn of 0.02V, allowing the high compliance voltage of 4.9V out of the 5V supply voltage. The 3 bit local DAC controls the current amplitude of anodic and cathodic pulses from the 8 bit global current DAC.



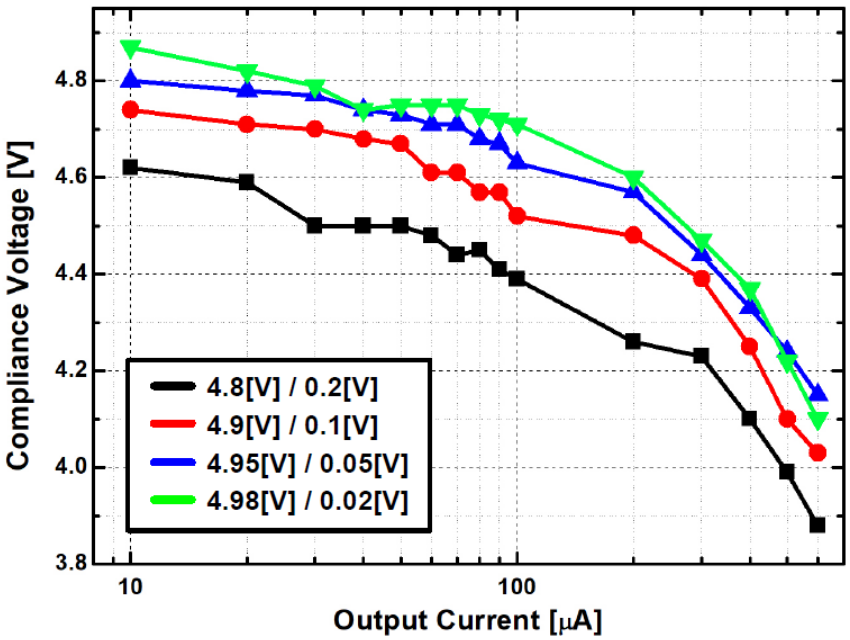


Fig. 3 shows the schematic of the bootstrapped switch for the passive CB. In a switch-based passive CB

to eliminate residual charge by shorting the working and reference electrodes, the time constant, directly related to the required discharging time, is related with the electrode-tissue impedance and the resistance of the switch. Therefore, a bootstrapped switch is employed instead of a conventional transmission gate switch for a faster passive CB. The voltage at the gate node of M6 is boosted to two times of the supply voltage while M2 and M7 are cascoded to prevent M1 and M8 from having gate-drain and gate-source voltages greater than VDD. The on-resistance of the bootstrapped switch is reduced to 19.56Ω from 43.48Ω of the conventional switch. Assuming discharging period of 8.9μs with 100μA current stimulation, the proposed passive CB scheme guarantees a residual charge of less than 1nC within a safe limit for the electrical current stimulation.

Measurement Results: The proposed electrical stimulator IC is fabricated in a 0.18μm standard CMOS process. The chip micrograph of the stimulator IC is shown in Fig. 4. The active area of the 1-channel stimulator and digital controller is 987.6μm × 815.7μm and 1.4mm × 1.4mm, respectively.

Fig. 5 shows the compliance voltage with respect to the output current amplitude from 10μA to 500μA when the reference voltages, Vrefp and Vrefn in Fig. 2 are applied with the 4.8/0.2V, 4.9V/0.1V, 4.95V/0.05V, and 4.98V/0.02V. The maximum compliance voltage is 4.9V with Vrefp and Vrefn of 4.98V and 0.02V at the output current of 10μA. At the output current of 50mA utilized in the in-vivo test, the stimulator satisfies the high compliance voltage of 4.75V.

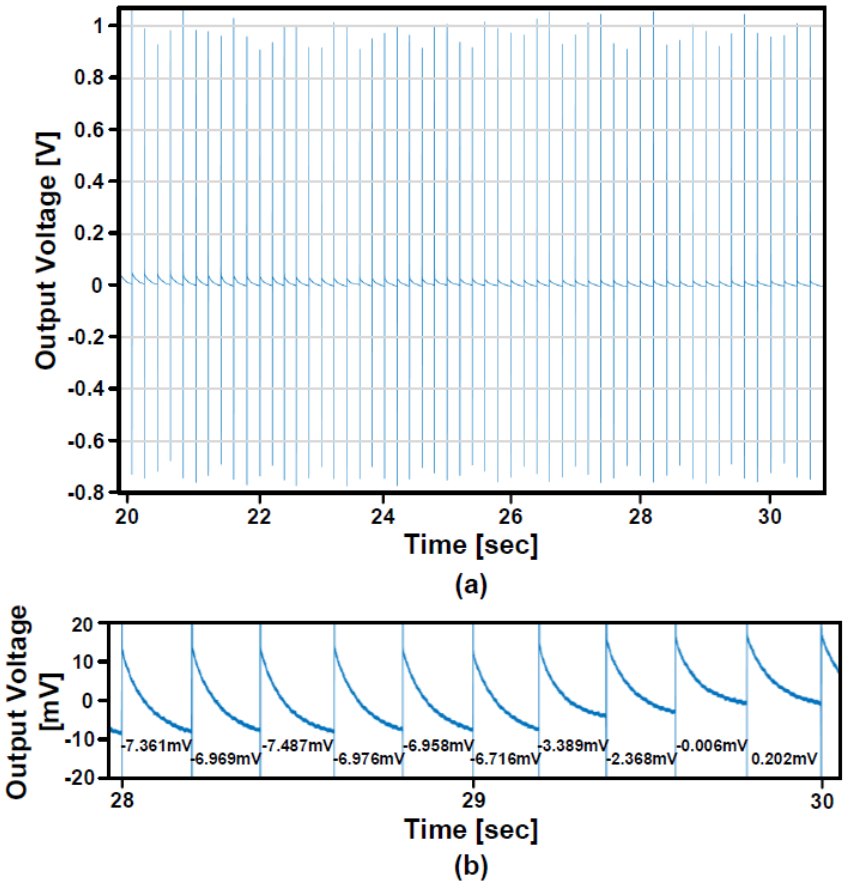
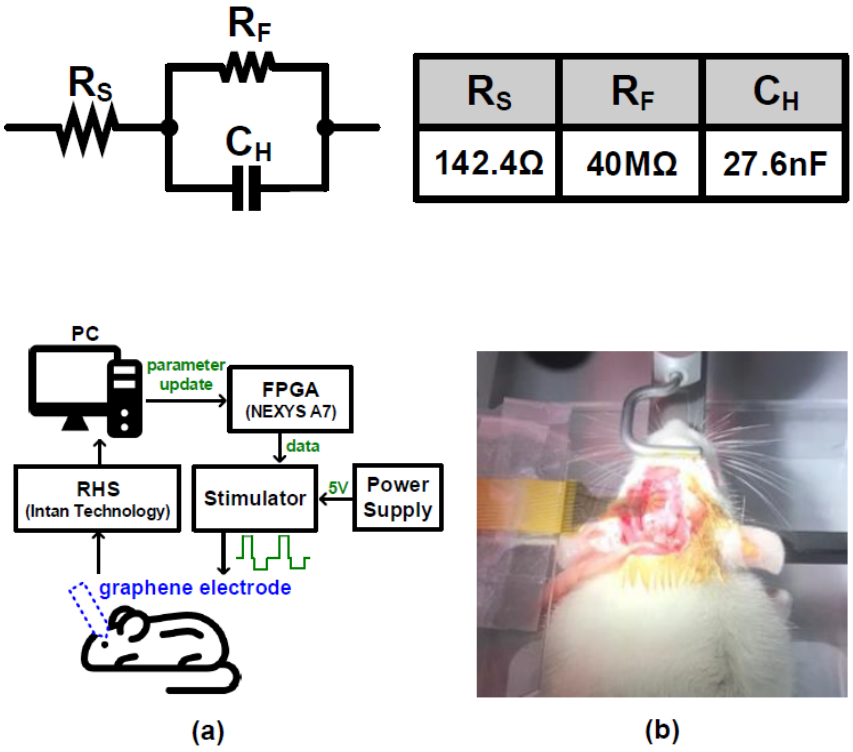


Fig. 6 compares the required discharge times of the conventional switch and the proposed bootstrapped switch when a monophasic stimulation pulse is applied to the circuit with the equivalent circuit model of the electrode-electrolyte interface using C_H=100nF, R_F=10MΩ, and R_S=10kΩ as in [4]. The monophasic pulse

is programmed with an amplitude of 400μA and a duration of 150μs, as shown in Fig. 6(a). Fig. 6(b) and (c) show the measured voltage across C_H when a conventional and bootstrapped switch is used, respectively. The discharge time of the conventional and bootstrapped switch is 86.9μs and 53.4μs, respectively, under the condition that the time from the start of CB until the residual charge of 1nC remains, which demonstrates that the bootstrapped switch is 39% faster in discharge time.

Fig. 7 shows the voltage between working and reference electrodes when the stimulation frequency is 5Hz with a bi-phasic current with 100μA amplitude and 100μs pulse width. The total stimulation time is 30 seconds, and Fig. 7(a) is the waveform for 10 seconds in the second half of the stimulation, and Fig. 7(b) is the zoomed waveform for 2 seconds in the second half of the stimulus. The voltage fluctuation generated by residual charges is at most 7.5mV as shown in Fig. 7(b), which corresponds to the equivalent residual charge of 0.75nC, which shows the proposed stimulation system is within 20 times less in the safe limit of 15nC [9].



In-vivo Test: In-vivo animal experiment in a rat is performed to verify the efficacy of the proposed stimulator for seizure suppression application. Fig. 8(a) shows the experimental environment for the test. The PC updates the stimulation parameters to the FPGA through the UART interface, followed by the SPI interface from FPGA to the stimulation IC. While stimulation pulses are applied to the rat, the commercial RHS recording platform (from intan technologies) records the ECoG signals, which is transmitted to the PC. As shown in Fig. 8(b), a micro-fabricated graphene electrode, which shows the impedance characteristics of Fig. 9, is directly attached to the somatosensory and/or motor cortical area of the brain for the experiment. Bicuculline is used to mimic seizure and is injected into the brain's somatosensory and motor cortex at a concentration of 15mM. Fig. 10(a) shows the entire waveform of bicuculline-induced seizure, which is suppressed through stimulation. Stimulation is performed with a frequency of 5 Hz, which is the most effective for seizure inhibition. Stimulation is continued for 40 seconds with the amplitude of 50μA and the pulse width of 10μs. Fig. 10(b-e) shows the waveforms when epilepsy, stimulation, inter-period of seizure to

stop, and suppression occurs, respectively. After 40 seconds stimulation, it takes 14 seconds to suppress the seizure.

A performance summary and comparison with other neural stimulators are presented in Table I. This work achieves high compliance per supply voltage through a low-cost standard CMOS technology. The 64-channel stimulator can be independently configured with a high resolution of 8 bits. In addition, for the feasibility verification, an animal test is peformed.

Conclusions: We present a 64-channel implantable current mode stimulator IC with a passive charge balancing scheme for seizure suppression. The proposed stimulator uses passive CB with a bootstrapped switch, demonstrating sub-nC charge-balanced operation. The regulated cascode driver satisfies a high compliance voltage ratio of 0.98 per supply voltage in 0.18 mm standard CMOS technology. The amplitude, pulse width, and activated channel of the stimulation waveform are variably adjusted with the SPI interface. In-vivo test shows the feasibility of seizure suppression through a 5Hz stimulation frequency with 50μA current amplitude and 10μs pulse width.

Acknowledgment:

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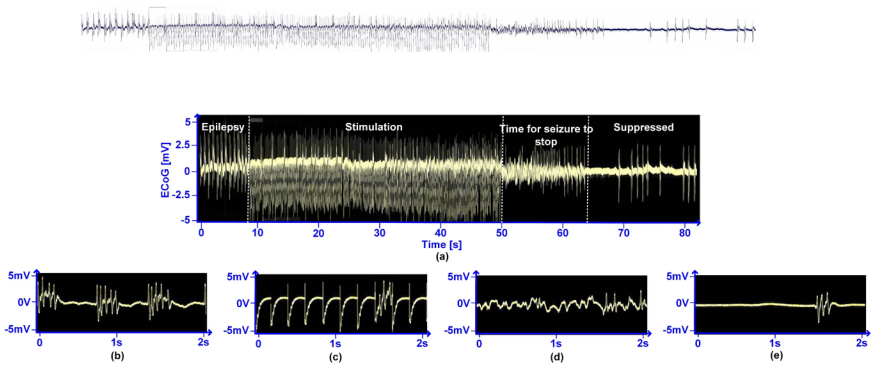

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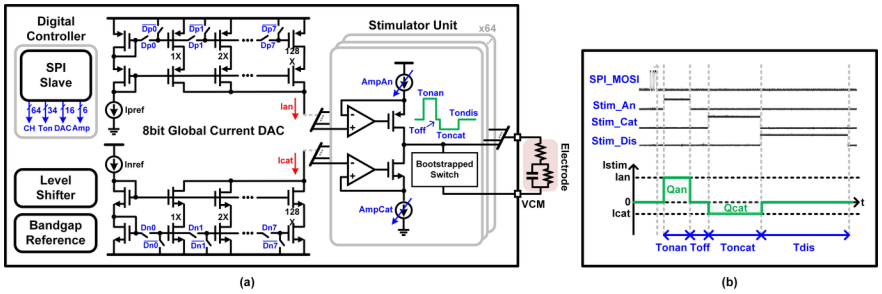

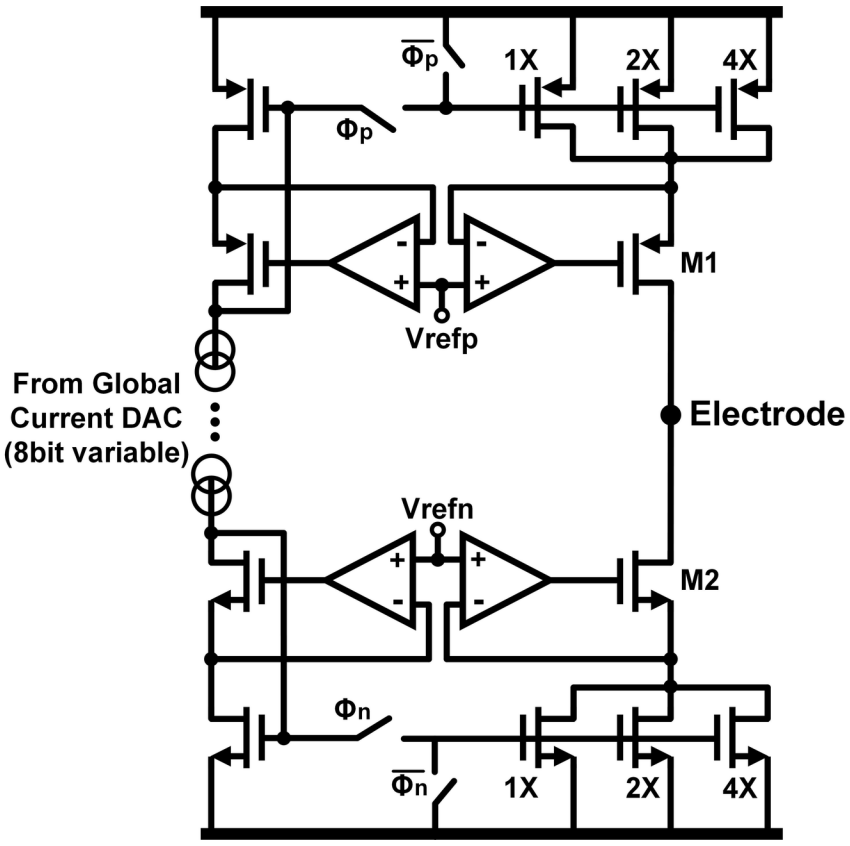

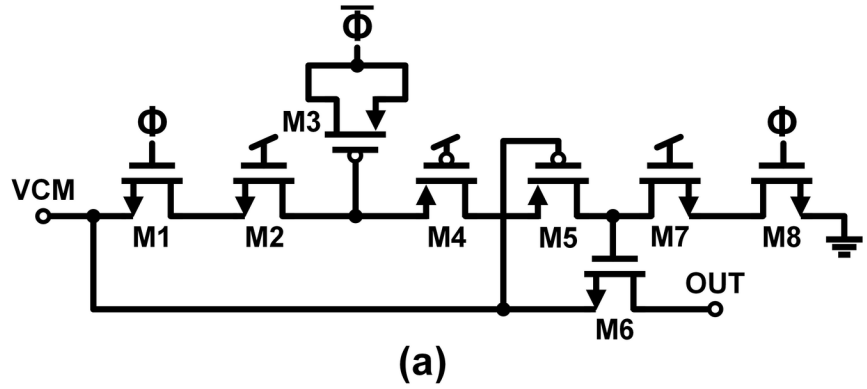

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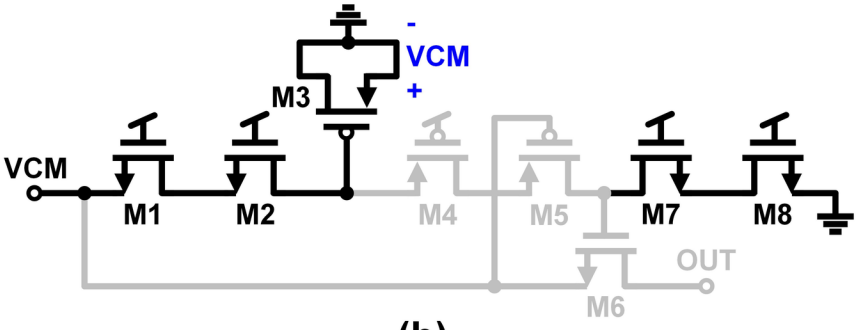

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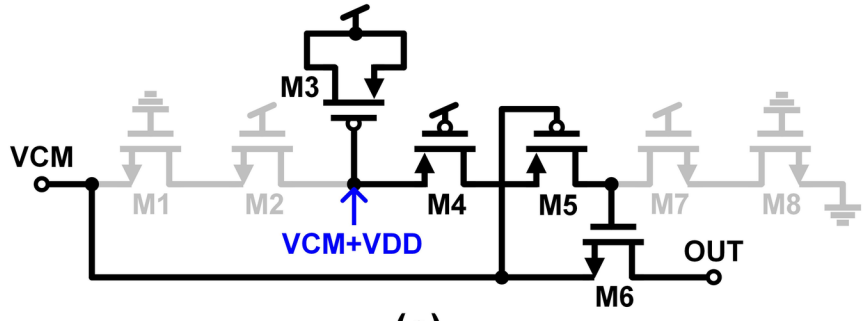

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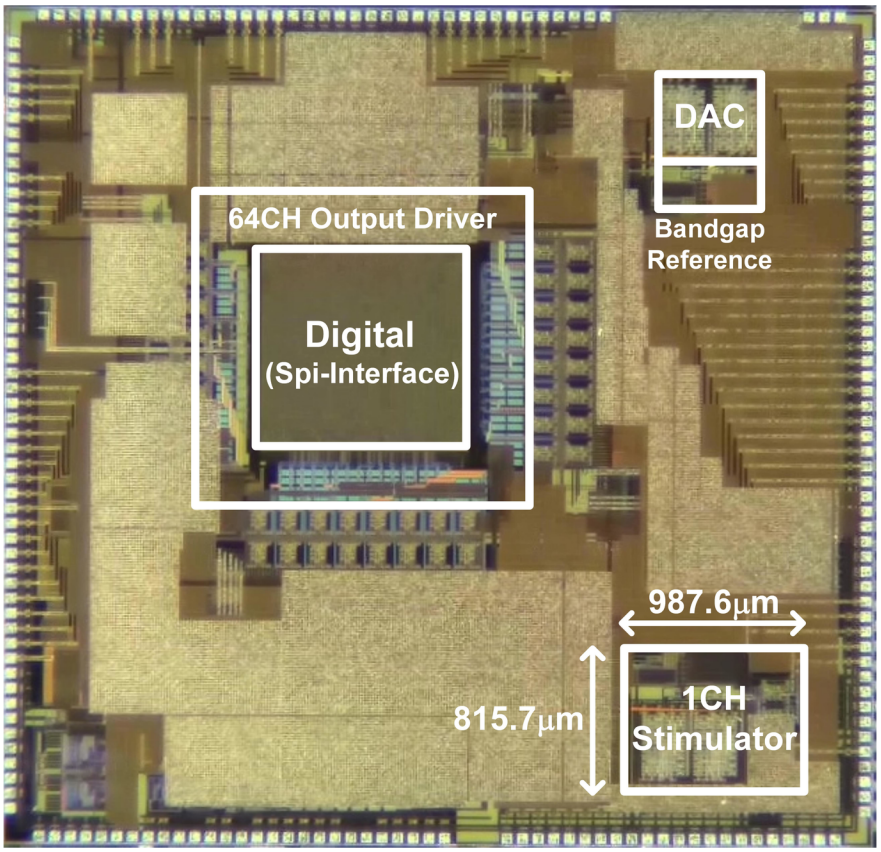

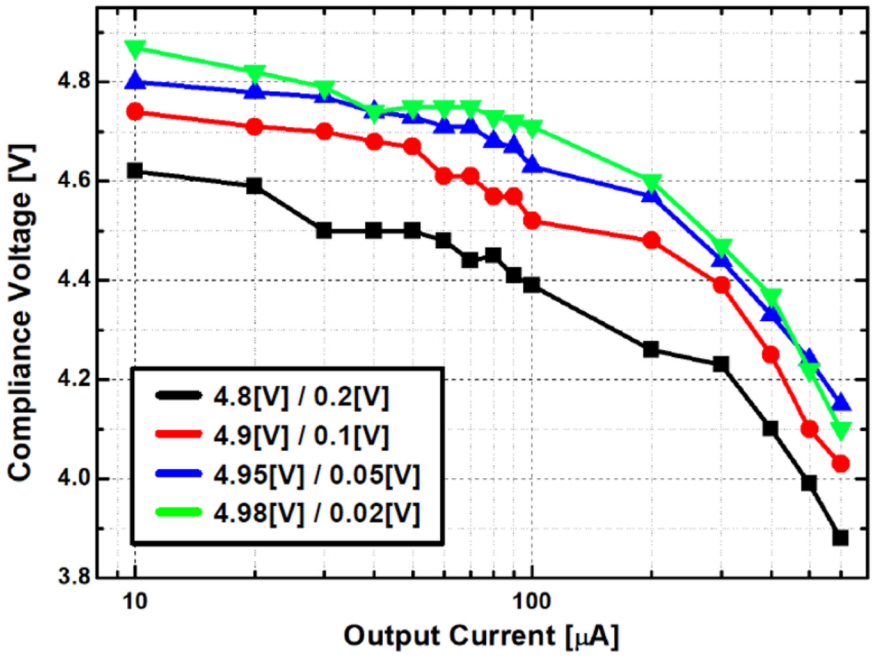

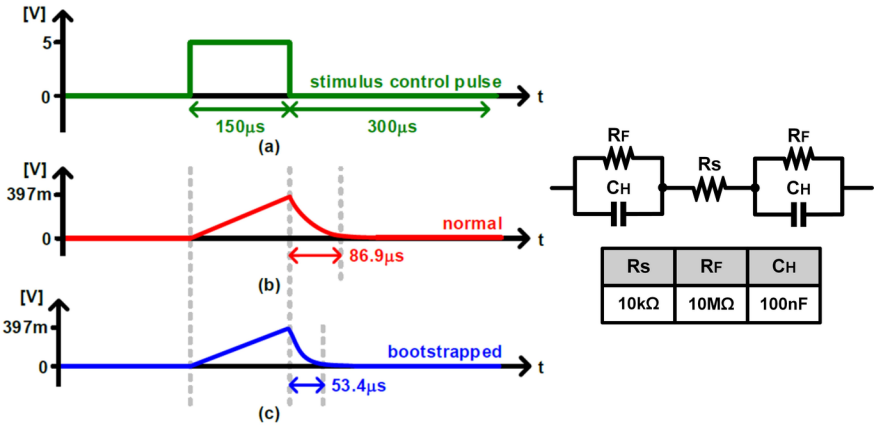

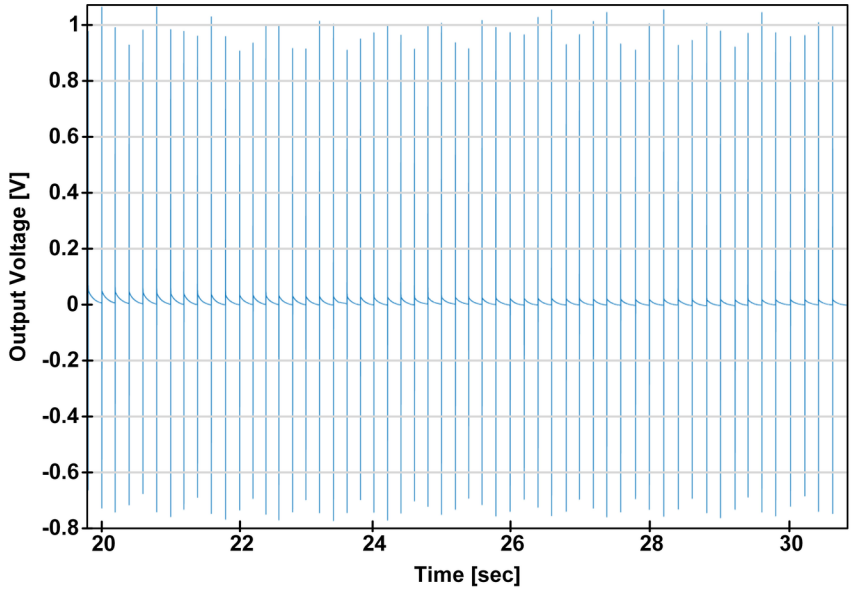

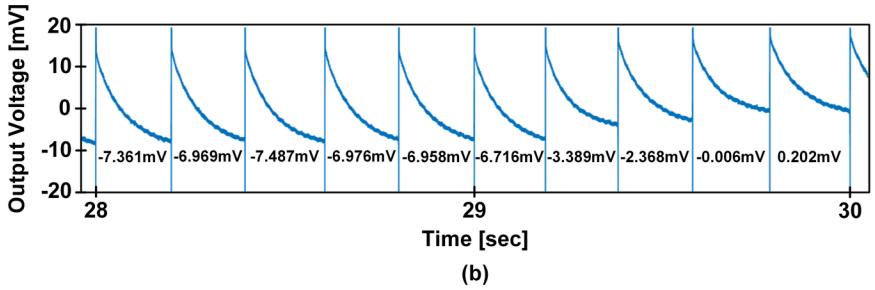

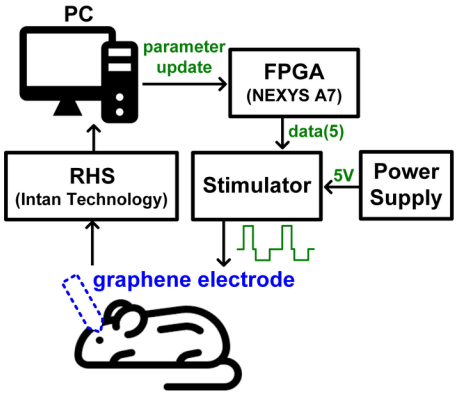

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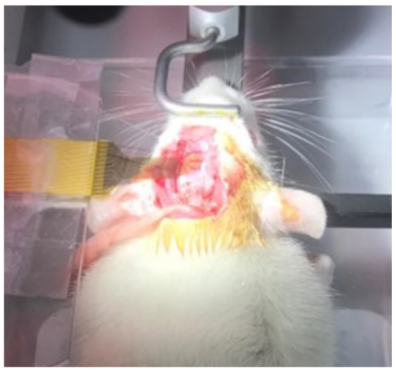

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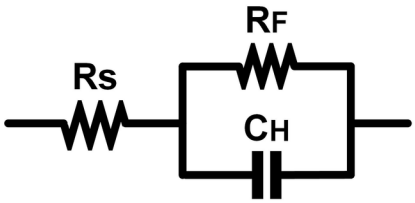

Rs	RF	CH
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