Enhancing Photodetection Efficiency of CMOS SiPMs using Virtual Guard Rings in a Standard 0.35 μm Process

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Abstract

In this letter, we introduce a design of virtual guarded SiPMs fabricated in a standard 0.35 μm standard complementary metal oxide semiconductor (CMOS) process. We compare the performance of these virtual guarded cells (VGC) to that of conventional cells with real guard rings, referred to as physical guarded cells (PGC). Specifically, we evaluate the photon detection efficiency (PDE) of both types of SiPMs. Our results demonstrate that the VGC SiPM outperforms the PGC SiPM, exhibiting a true PDE of (22.5 ± 0.5) %, which is significantly higher than the PDE of (10.9 ± 0.3) % obtained for the PGC SiPM. The superior PDE of the VGC SiPM is attributed to a larger active or photosensitive area due to the virtual guard rings and a thinner n-layer in the photosensitive region.

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In this letter, we introduce a design of virtual guarded SiPMs fabricated in a standard 0.35 µm standard complementary metal oxide semiconductor (CMOS) process. We compare the performance of these virtual guarded cells (VGC) to that of conventional cells with real guard rings, referred to as physical guarded cells (PGC). Specifically, we evaluate the photon detection efficiency (PDE) of both types of SiPMs. Our results demonstrate that the VGC SiPM outperforms the PGC SiPM, exhibiting a true PDE of (22.5 ± 0.5) %, which is significantly higher than the PDE of (10.9 ± 0.3) % obtained for the PGC SiPM. The superior PDE of the VGC SiPM is attributed to a larger active or photosensitive area due to the virtual guard rings and a thinner n-layer in the photosensitive region.

Introduction: Silicon photomultipliers (SiPMs) are highly sensitive detectors for applications that require low-level light detection, with the ability to detect single photons while exhibiting high gain, low noise, and excellent timing resolution [1]. SiPMs consist of arrays of single photon avalanche diodes (SPADs) and are widely used in various fields, such as medical imaging [2], nuclear physics [3], and high-energy physics [4].
Researchers integrate SiPMs into standard complementary metal oxide semiconductor (CMOS) processes to facilitate the integration of sensing elements and readout circuits on a single chip, thereby enhancing the performance and functionality of SiPMs.
However, one of the key characteristics of these detectors are their photon detection efficiency (PDE), which is defined as the ratio of the number of detected photons to the number of incident photons. The PDE of SiPMs is given by the product of four factors [5]:

$$PDE = \epsilon \cdot IQE \cdot P_{trig} \cdot (1 - R) \tag{1}$$

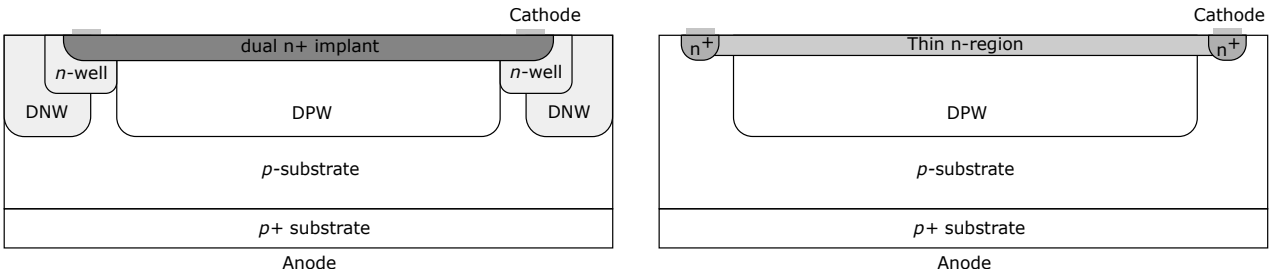
The geometrical efficiency (ϵ) refers to the proportion of the active area that is photosensitive. The internal quantum efficiency (IQE) of SiPMs refers to the probability of generating a free photoelectron in the photosensitive area of the SiPM from an incident photon. The breakdown trigger probability (P_{trig}) describes the process of multiplying the generated photoelectron through an avalanche breakdown. Additionally, the optical input reflection coefficient (R) represents the fraction of incident photons that are reflected by the SiPM surface.
Various techniques have been proposed to improve the PDE of SiPMs and SPADs in standard CMOS processes. One such approach involves manipulating the depth of the multiplication region to increase the PDE [6]. Other researchers try to reduce the thickness of the dead layer at the junction interface to increase the breakdown trigger probability [7]. Other techniques try to optimize ϵ and the geometry of the APD cells, for example, by replacing physical guarding with virtual guard rings for individual SPADs [8].
The technique of virtual guard rings is employed to enhance the active region of each SPAD and mitigate the effects of edge breakdown [8] [9]. Rather than employing physical guard rings, virtual guard rings are created through the overlapping of a thin, lightly doped n-region with a heavily doped n+ region, which is connected to a metal contact that serves as the cathode. The adoption of a lightly doped n+ region in combination with a slightly diminished p-well width results in a decreased electric field at the edges to prevent edge breakdown [10].
While the implementation of virtual guard rings in custom processes has gained widespread acceptance [11], their successful realization in standard CMOS technology remains a challenging task.
In this study, we undertake a detailed analysis of the design of two SiPMs consisting of 254 microcells fabricated using a 0.35 µm process technology. One of the SiPMs incorporates physical guarded cells (PGC), while the other employs a approach using virtual guarded cells (VGC) without real guard rings. The SiPMs are fabricated using standard 0.35 µm CMOS technology by X-FAB foundry.

Device Structure: The cross-sectional view of both kinds of SPADs is depicted in Figure 1a and 1b. Each SPAD of both detectors had a microcell pitch of 54 µm. The PGC SPAD is fabricated with a pn-junction consisting of a deep p-well (DPW) and a highly doped dual n+ implant. In order to mitigate edge breakdown effects, a conventional guard ring comprising an n-well and a deep n-well (DNW) was implemented [11]. The introduction of the DNW was selected to ensure the prevention of edge penetrations. Nevertheless, this additional n-region does not adversely affect the photosensitive area. The contact was positioned on the edges of the dual n+ implant, while the anode was formed by a p+ substrate located beneath the p substrate on the backside of the SPAD. The design of guardrings in standard CMOS processes is limited in dimensions by the constraints imposed by the fabrication facility and design rules.
The VGC technology utilizes an approach in a 0.35 µm CMOS to guard against corner junction breakdown without the use of physical guard rings. Instead, the VGC incorporates a thinner, less heavily doped n-type layer that overlaps with an n+ layer connected to the cathode. Based on the breakdown voltages, we suspect that the tails of the dopant profile are smoother for n+. The VGC eliminates the need for physical guard rings, which enables an 44 % expanded light sensitive region between the thin n-region and the DPW, thereby enhancing the PDE. However, there was a potential risk of complete depletion of the thin n-type region due to the lower doping concentration and thinner layer. The anode is connected to the p+ layer on the rear side of the SiPM, and both the VGC and PGC SPADs were passively quenched by a polysilicon resistors with a value of $R_q = 430\,\text{k}\Omega$. We did not employ any specific optical window processing options, which may result in a significant reduction in light intensity (up to approximately 10 %) even prior to photon penetration into the semiconductor photosensitive area.

Table 1. Standard characterization parameters for the PGC and the VGC SiPM designs

	PGC	VGC
Breakdownvoltage:	28.2 V	26.2 V
XT:	2.5 %	4 %
DCR:	2.8 $\frac{\text{Mhz}}{\text{mm}^2}$	2.2 $\frac{\text{Mhz}}{\text{mm}^2}$
CDN:	48 %	55 %
Gain:	2.25 x 10^6	4.45 x 10^6
RC-time:	7.2 ns	16.3 ns
Operating range:	1 V - 4 V	1 V - 2.5 V

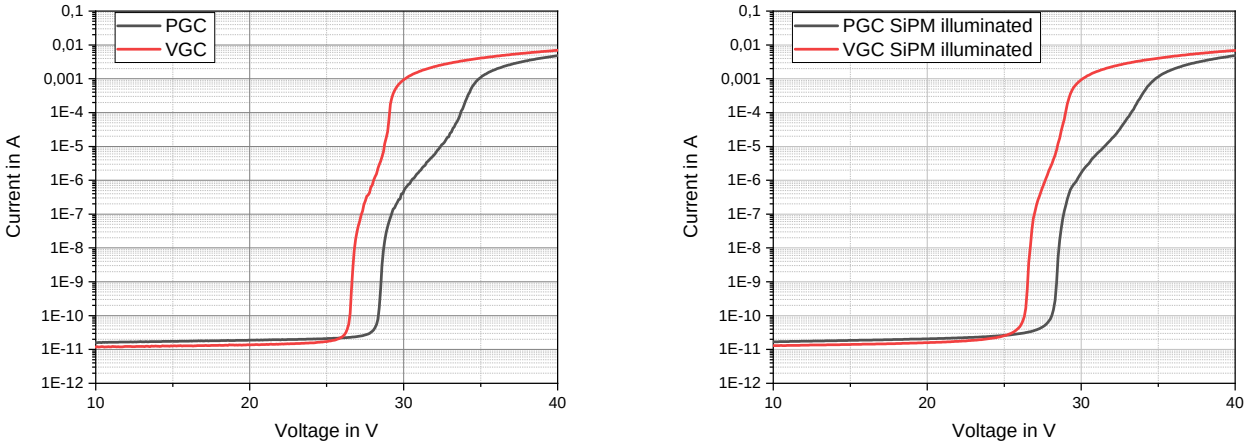
Standard Characterization of CMOS SiPMs: For standard characterization, the current-voltage (IV) curves were obtained in both the presence and absence of a small amount of light, as depicted in Figure 2. It is noteworthy that a relatively gradual breakdown can be observed on the IV curves, which is likely attributed to the specific geometry and size of the CMOS SiPMs being investigated. The PGC and VGC SiPM exhibit breakdown voltages of 28.2 V and 26.2 V, respectively, and a punch-through voltage (which defines the second breakdown) of 35 V for the PGC and 29.5 V for the VGC with a variation of 0.1 V. The operational range for both SiPMs is up to 4 V overvoltage (OV) for the PGC and up to 2.5 V OV for the VGC.
Further standard parameters regarding SiPM performance are presented in Table 1, with measurements made at an OV of 2 V. The two SiPMs exhibited comparable performance, with some noticeable differences. The VGC SiPM showed a higher crosstalk rate (XT) of 4 %, which is attributed to the closer proximity of its cells. Both detectors also showed high correlated delayed noise (CDN) of approximately 50 %, including delayed crosstalk and afterpulsing events. It is challenging to differentiate between the two effects, but analyzing the magnitude and simultaneous timing of pulses can estimate the share of delayed crosstalk. We estimated that about 70 % of the pulses are delayed crosstalk pulses.



(a) *Cross section of the PGC SiPM*

(b) *Cross section of the VGC SiPM*

Fig 1 *Cross-sectional view of the PGC (a) and VGC (b) SiPMs, illustrating their internal structure and design*



(a) *IV-curve of PGC and VGC in complete darkness*

(b) *IV-curve of PGC and VGC illuminated*

Fig 2 *In this figure, we can see two IV-curve graphs, one for PGC (black) and the other for VGC (red) SiPM. The first graph (a) shows the IV-curve measurements of both SiPMs taken in complete darkness. The second graph (b) illustrates the IV-curve measurements of both SiPMs when exposed to light.*

The VGC SiPM exhibits a higher gain compared to PGC, as its larger photosensitive area is achieved through a larger area of pn-junction, resulting in higher capacitance. In turn, the PGC SiPM exhibited a lower value of recovery time due to its lower diode capacitance. Both sensors exhibited high dark count rates (DCRs), with the PGC SiPM having a dark count rate of 2.8 $\frac{\text{Mhz}}{\text{mm}^2}$ and the VGC SiPM having a slightly lower dark count rate of 2.2 $\frac{\text{Mhz}}{\text{mm}^2}$.
The significant difference between the two SiPMs is their operating range. The VGC SiPM has an operating range which is roughly half that of the PGC SiPM. The reduced operating range of the VGC SiPM may be attributed to its tendency to experience edge breakdown at a OV as low as 3 V. Overall, the operating range of both SiPMs is not too wide and is constrained by elevated CDN rates.

Photon Detection Efficiency Measurement: The setup for our measurements was proposed and described in [5]. We performed measurements to determine the true PDE of our designed CMOS SiPM, with excluding XT and APP. For illumination, we used the 463 nm wavelength. The temperature was maintained at 293.15 K. The results of the PDE measurements are depicted in Figure 3. The error bars denote the standard error of the mean value, obtained from the three measurement cycles. The presented PDE data accounts for CDN effects (i.e. they are excluded). In order to obtain precise and reliable PDE values, a voltage range of 1.75 V OV to 2.25 V OV was chosen for the measurements. This range was determined by taking into account several factors, including pulse height, noise factors, and the operating range of the VGC SiPM. The major limiting factor that affects the PDE within this voltage range is the DCR per unit area of the detector and the CDN.
As shown in Figure 3, the PDE values of both SiPM increase proportionally with increasing OV. The PGC SiPM achieves a maximum PDE of (10.9 ± 0.3) %, while the VGC SiPM attains a PDE more than twice as high, at (22.5 ± 0.5) %, both at an OV of 2.25 V.

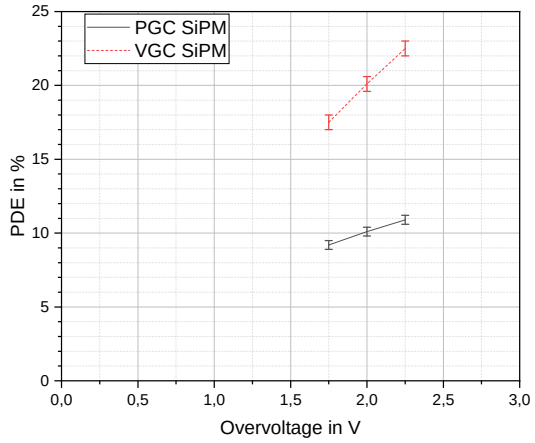


Fig 3 *The PDE measurement results for both PGC and VGC CMOS SiPMs are presented, with their dependence on overvoltage.*

Discussion: Our findings demonstrate that our virtual guarded SiPM outperforms the conventional SiPM in terms of PDE by a factor of 2.06 at an OV of 2.25 V. This increase in PDE can be attributed to two

primary factors, if we note Equation 1. Firstly, our approach leads to a 44 % increase in the photosensitive area, resulting in a correspondingly higher ϵ and PDE respectively. Secondly, the thinner and less heavily doped thin layer of the VGC SiPM enabled a wider absorption area, leading to an increase in P_{trig}.

Our results also indicate that both SiPMs exhibit similar parameters in standard characterization. Nevertheless, it is noteworthy that the VGC SiPM displays a restricted operational range, as evidenced by the pronounced slope in the IV curves depicted in Figure 2 (b). This characteristic steepness within the operating range causes the current to become independent of the light effect at a relatively low voltage of 29.5 V.

Additional research is necessary to address this issue and expand the operational range, which could result in a significantly higher PDEs, particularly if we extrapolate the PDE enhancement with respect to the OV in Figure 3 beyond several volts. The significant increase in PDE with the OV has already been shown by other studies [12] [13].

Furthermore, our PDE measurements did not cover a wider range of wavelengths, and literature indicates that PDE reaches its peak at approximately 420 nm in CMOS technology. In the context of these points, PDEs of up to 40 % have already been demonstrated [12] [14]. This, in turn, suggests that a significantly higher PDE could be expected from our SiPM after optimisation of cell's design, using an optical window with anti-reflective coating and illumination with optimal wavelength.

Conclusion: In this letter, a virtual guarded SiPM has been presented in standard CMOS 0.35 µm, and its performance has been compared to a conservatively guarded SiPM in the same technology node. The results of our approach show a remarkable increase in the PDE from (10.9 ± 0.3) % to (22.5 ± 0.5) % at an OV of 2.25 V and a wavelength of 463 nm, which is a factor greater than 2. Both SiPMs have exhibited similar parameters during standard characterization. However, the operational range of the VGC SiPM is limited, which require further investigation to address the issue. By increasing the operational range, an even better PDE can be achieved. Future research could concentrate on expanding this approach by optimizing the virtual guard rings through simulations while abiding by the given constraints and increasing the absorption area.

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