Invisible ZnO-based Memristor Universal Logic for Reconfigurable Electronics

Chen Hua, Sridhar Chandrasekaran, Member, IEEE, Shan Gao, Dimitra G. Georgiadou, Member, IEEE, Zohreh Hajiabadi, and Firman M. Simanjuntak, Senior Member, IEEE

***Abstract*— The implementation of two-terminal memristors could decrease the dependency on the transistors in logic circuits, enabling high-density circuits and reducing power consumption due to the memristor's smaller feature size and non-volatility, respectively. We propose universal logic function designs using ZnO-based transparent memristors. A highly accurate fitting of set and reset curves is achieved by employing Verilog model and used for circuit-level simulations. OR, NOR, NAND, and AND gates can be designed by simply tuning the memristor and pull-up resistor while using a similar circuit configuration. Based on this facile configuration, more complex circuits, such as XOR and XNOR gates as well as half-adder and half-subtractor combinational logic circuits can be achieved. This work highlights a promising alternative for reconfigurable logical integrated circuits.**

***Index Terms*— Compact model, AND, NAND, OR, NOR, XOR, XNOR, logic gates, transparent electronics, reconfigurable electronics.**

I. INTRODUCTION

Today's logic circuits are based on transistor technology. However, transistor architecture is facing scalability limits, hindering the realisation of ultra-high dense chips[1]. A transistor requires a continuous supply of power for its operation (volatile), which means that as more transistors are added to logic circuits, the power consumption needed to run the computation is increased. Moreover, transistors are not resilient against high-energy radiation, which makes them unsuitable for long-term missions in harsh environments, such as in space and at high altitudes[2]. Small, low-powered, and rad-hard (SLR) circuits are important metrics to reduce the cost of deployment and maintenance in such environments. Hence, the circuits are often designed to have less number of transistors, whenever possible, to meet the SLR constraint.

Memristor is an emerging nonvolatile memory technology that offers great promise for next-generation data storage and in-memory computing applications[3]. The memristor has been introduced as the fourth fundamental circuit element and has a unique capability of restoring its resistance upon programming without the necessity of continuous power supply. Furthermore, the memristor is a highly scalable and rad-hard circuit element[2].

Efforts have been made to design logic circuits using memristors, such as memristor-based material implication (IMPLY)[4], memristor-ratioed logic (MRL) [5] and memristor-aided logic (MAGIC)[6]. However, most designs developed on these models have limited capability in cascading the gates, require many operation steps and fan-out structures, and the switching characteristics are demonstrated solely through theoretical approaches and not from actual devices[7], [8], [9]. In this work, we investigate the feasibility of a ZnO-based transparent memristor for making Boolean logic functions (OR, NOR, NAND, AND, XOR and XNOR) by adopting Stanford and Peking universities' compact model and propose facile and reliable designs to realise the universal logic functions.

II. METHODS

An 80 nm highly transparent ZnO film was grown on a commercial ITO-coated glass; the ITO thickness is 300 nm and is used as a bottom electrode (BE) contact. The ZnO was grown by an RF Sputtering system with a sputtering power of 80 W under argon and oxygen gas ratio of 12:6 sccm. Next, a transparent ITO top electrode (TE) was deposited on top of ZnO using a metallic shadow mask having 150 μm diameter and 150 nm thickness. The schematic of the fabricated ITO/ZnO/ITO devices is depicted in Fig. 1(a). The electrical characteristics of the transparent device were measured using an Agilent B1500 semiconductor parameter analyser; voltage bias was applied on the TE, and BE was grounded. The transparency of the device was measured using a Shimadzu UV-2600i UV-Vis absorption spectrometer, and it was found that the memristor structure has a high transparency of approximately 75% in the visible region, as shown in Fig. 1 b). The ZnO compact model and logic circuits simulations are conducted using Agilent Advanced Design System software, and the Stanford - Peking (SP) compact model [10], [11] was used to model the ZnO-based memristor.

III. RESULT AND DISCUSSION

The resistive switching characteristics of the memristor are actuated by applying a positive voltage sweep to obtain electroforming, as shown in Fig. 1(c). Electroforming is achieved by sweeping the device to 2.2V with 5 mA as current compliance. The ITO/ZnO/ITO transparent memristor is then swept back to HRS by applying a negative sweep voltage of -2.4 V (reset). Similarly, the memristor is again switched from

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C. Hua, S. Gao, D. G. Georgiadou, Z. Hajiabadi, and F. M. Simanjuntak are with the School of Electronics & Computer Science, University of Southampton, Southampton, United Kingdom. (email: ch4u22@soton.ac.uk , sg4g22@soton.ac.uk, d.georgiadou@soton.ac.uk, z.hajiabadi@soton.ac.uk, f.m.simanjuntak@soton.ac.uk)

S. Chandrasekaran is with the School of Electronics Engineering, Vellore Institute of Technology, Chennai, Tamil Nadu, India 600127 (email: sridhar.c@vit.ac.in; sridharc9020@gmail.com)

HRS to LRS by applying a positive voltage sweep of 1.2 V with a current compliance of 5 mA (set). ITO/ZnO/ITO memristor exhibits reproducible analogue switching behaviour with stable switching, as shown in Fig. 1(d).

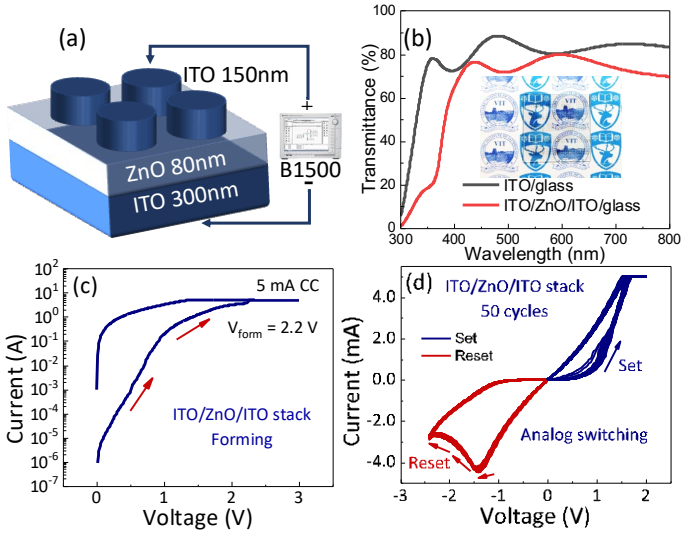

Fig. 1. a) Schematic of the transparent memristor device structure and testing biasing; (b) Transmittance spectra of the ZnO film on glass and of the fully transparent memristor device; (c) Forming curve of the ITO/ZnO/ITO device, (d) The typical switching characteristics of the device, showing 50 consecutive cycles of set and reset processes. Inset in (a) shows the photograph of the fabricated memristors on a glass substrate.

Fig. 2(a) shows the equivalent circuit model of the metal oxide resistive switching memory with the top and bottom electrode contacts supported by the parasitic resistances R_{TE} & R_{BE}, respectively. Similarly, the Rh represents parasitic resistance between the electrodes. The SP compact model is used for the initial current-voltage fitting of the memristor equivalent circuit. Fig. 2(b) shows the transient response on applying a set pulse of 2 V and 20 µS pulse width (with 20 µS rise and fall time). Similarly, to obtain reset operation, a pulse of -2.2 V amplitude and 20 µS pulse width (with 20 µS rise and fall time) is applied.

Fig. 3(a) shows the I-V switching during set operation with the experimental and compact model fitting of the transparent device. The ZnO transparent device exhibits analogue switching behaviour with a memory window spanning ~2 orders of magnitude, which agrees well with the fitting of the SP compact model. Similarly, the reset operation is achieved by applying -2.2 V, as depicted in Fig. 3(b), and the compact model shows an accurate fit with the experimental data of the ZnO-based RRAM.

To realise the logical OR operations, the two memristors are connected in parallel, with the BE connected to the load resistance (R_L) and the TE connected to pulsed voltage sources (V_A & V_B), as shown in Fig. 4(a). The pulsing sequence operation of the OR Logic function is shown in Fig. 4(b) with a 2-bit logical OR operation. Similarly, the NOR logic operation is conducted by introducing the CMOS inverter to the OR logic to achieve NOR operation, as shown in Fig. 4(c). We used the ASU 16 nm PTM library for the inverter logic operation. Fig. 4(d) shows the time domain logical voltage switching for the 2-bit NOR logical operation with various logic state evolution using a pulsing scheme for both the input bits. Fig. 4(e) shows the schematic of the NAND logic operation with a change in the load resistance of 60 Ω, which allows the logic state transition using logical NAND operation. The time domain logical switching curve of the NAND logic gate is shown in Fig. 4(f), showcasing reproducible NAND logic switching by adjusting the state load resistance. Similarly, the AND gate can be realised by connecting the NAND circuit with an inverter (Fig. 4(g, h))

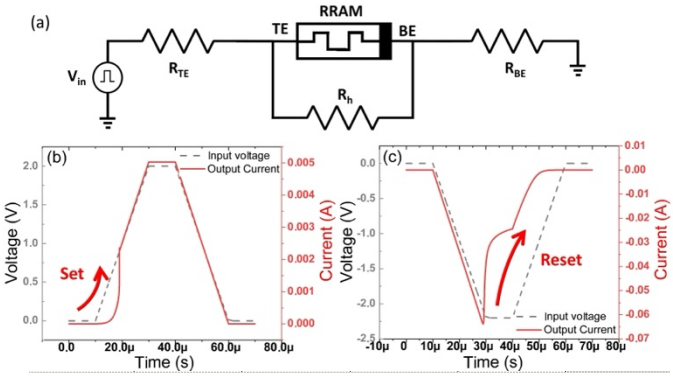

Fig. 2. (a) Equivalent circuit of the ZnO-based memristor; (b) & (c) Transient response of set and reset on applying 2 V and -2.4 V pulses, respectively.

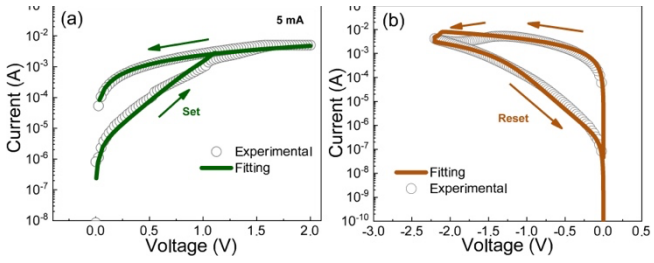

Fig. 3. (a) & (b) Set and reset I-V fitting of ITO/ZnO/ITO memristor.

The inverter using 16 nm ASU PTM has a width of 64 nm and

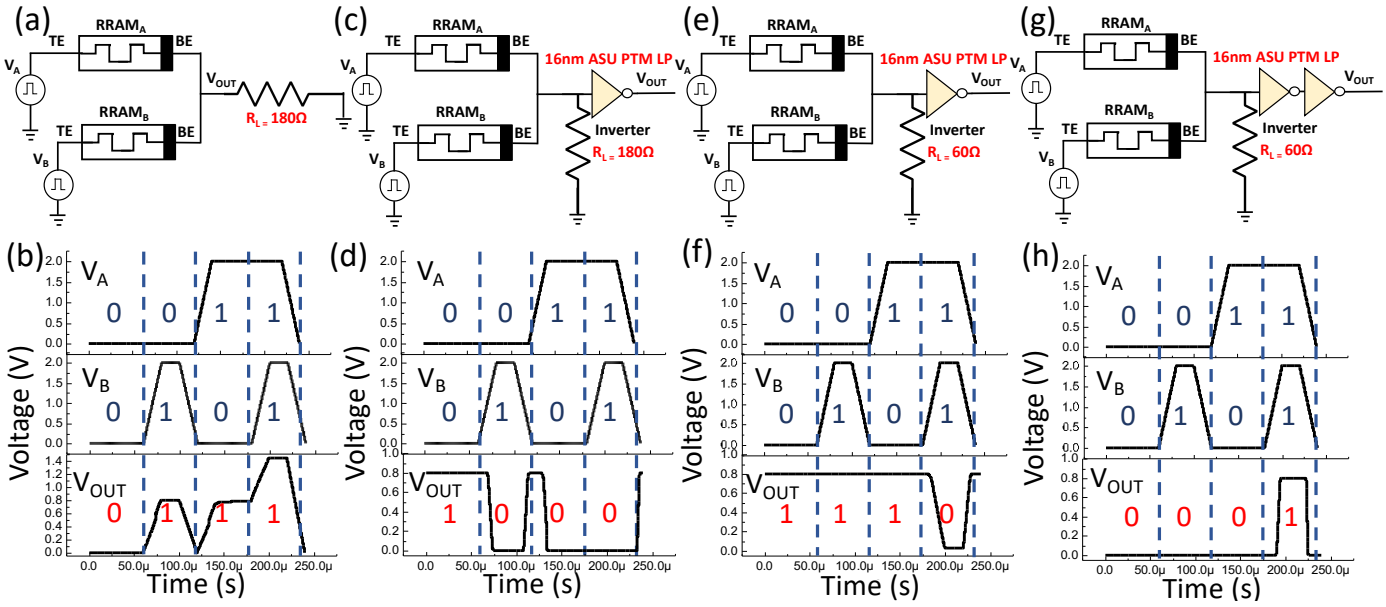

Fig. 4 Schematics and V-t curves of (a,b) OR, (c,d) NOR, (e,f) NAND and (g,h) AND logic gates.

a length of 16 nm for the PMOS transistor. The NMOS transistor has a smaller width of 32 nm and a length of 16 nm, as shown in Fig. 5(a). I-V characteristics of the ASU inverter logic are shown in Fig. 5(b), and the inverter is tuned to operate with a threshold voltage of 0.4 V, while the threshold voltage of the inverter plays a crucial role in the transition of NOR to NAND logic operation. V_{ab} is measured at the load resistance point, which is depicted as the red star that is crucial for determining the critical voltage ($V_{critical}$). Fig. 5(c) shows the schematic diagram of the NAND or NOR logic with minor changes in the load resistance influencing the transition, which is advantageous over a conventional logic circuit.

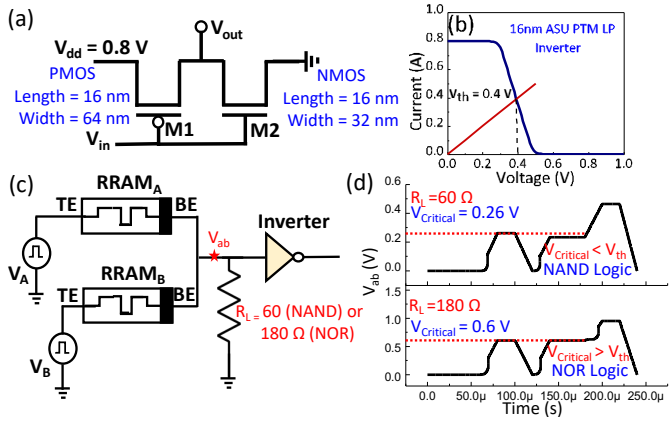

Fig. 5. (a) Inverter circuit based on 16 nm ASU PTM library; (b) I-V of the CMOS inverter with Vth of 0.4 V; (c) Schematic of the NAND and NOR logic with varying load resistance; (d) NOR to NAND transition using Vcritical and Vth based logic.

During NAND Logic operation, the $V_{critical}$ is 0.25 V with a load resistance of 60 Ω, as when the $V_{critical} < V_{th}$ the circuit operates in NAND Logic, as shown in Fig. 5(d). Also, the NOR logic can be realised by keeping the load resistance of 180 Ω with $V_{critical} > V_{th}$, as shown in the same figure. The critical voltage engineering by resistance modulation plays a major role in the transition of the operating mode from NOR to NAND. The major benefit of using this method to realise the universal logic is low-cost cost, fab-friendly alternative technology with minimal changes in the circuit-level design. This approach of realising the universal logical gate reduces the number of transistors involved and improves the scalability of large-scale integrated circuits. The same approach can be used to achieve more complex logical operations, such as XOR and XNOR, as illustrated in Fig. 6.

To achieve the XOR operation (Fig. 6(a)), the output of the OR logic (Fig. 4(a)) is connected to an nMOS transistor, while two parallel flipped memristors are connected to a pMOS transistor and both MOSFETs are connected in parallel with an nMOS transistor. The circuit of the XOR gate and the output are shown in Fig. 6(b). Meanwhile, for the XNOR logic function, the output of the flipped memristors in parallel is connected to an nMOS transistor, and the output of the OR logic gate is connected to a pMOS transistor. The pull-up load for the parallel memristors is lower than the XOR gate (Fig. 6(c)) to produce the correct output, as depicted in Fig. 6(d).

Compared to the typical transistor-to-transistor logic designs, the proposed design in this work is much simpler. We further examined the feasibility of our designs to execute half-adder/subtractor functions by combining an AND (Fig. 4g) and an XOR (Fig. 6a) gate, and the result is shown in Fig. 7. The half-adder function was simulated successfully, showing the addition of two one-bit binary numbers (Fig. 7(a,b)). Similarly, a one-bit subtractor function can be executed without debit inputs, which consists of an AND logic gate, XOR logic gate and inverter (Fig. 7(c,d)).

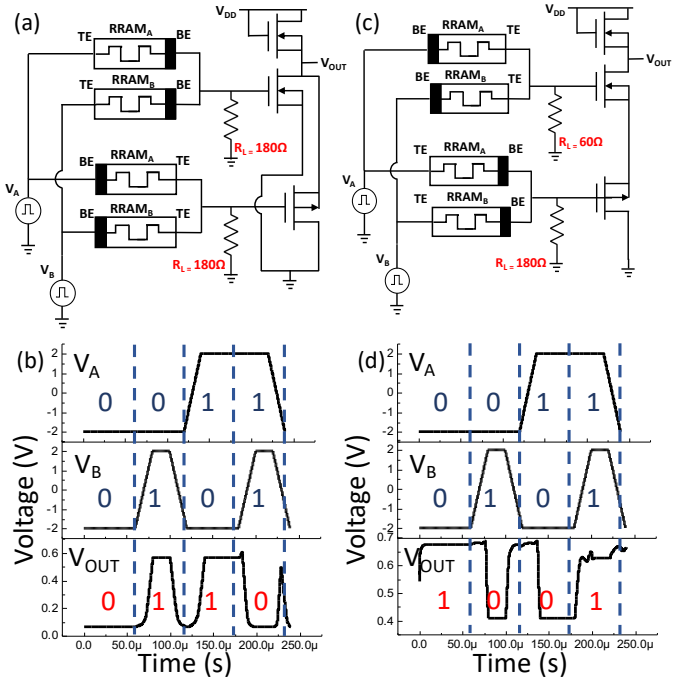

Fig. 6 Schematic and V-t curve of (a, b) XOR Logic and (c, d) XNOR Logic.

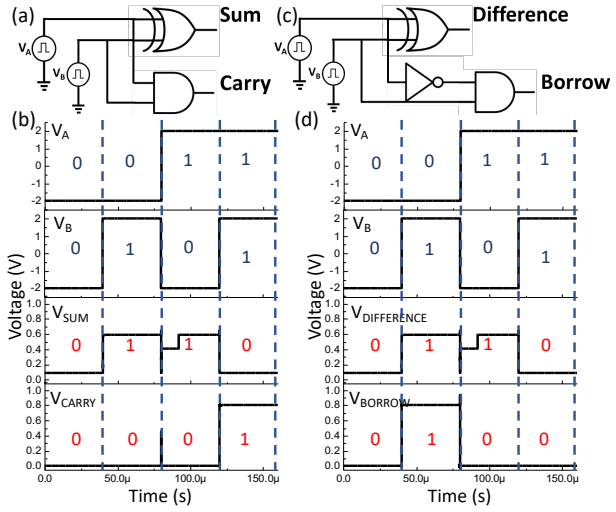

Fig. 7 Schematic and V-t curve of (a,b) half-adder; (c,d) half-subtractor.

V. Conclusion

In this study, we fabricated the ZnO-based transparent memory and their resistive switching is modelled using the SP compact model. We have explored the feasibility of realising the gated logic functions OR, NOR, NOR, NAND, AND, XOR and XNOR with such memristors. The transition of logical operation from NOR to NAND can be done by simply varying the load. We further proved that our designs are suitable for simulating combinational logic circuits. Fabrication of the hardware of these logic circuits and the derived ALU is currently underway and will be reported in the future. This study provides insight into memristor-based large-scale logical circuits for next-generation computational systems.

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